

005007 4703950

FIG. 2

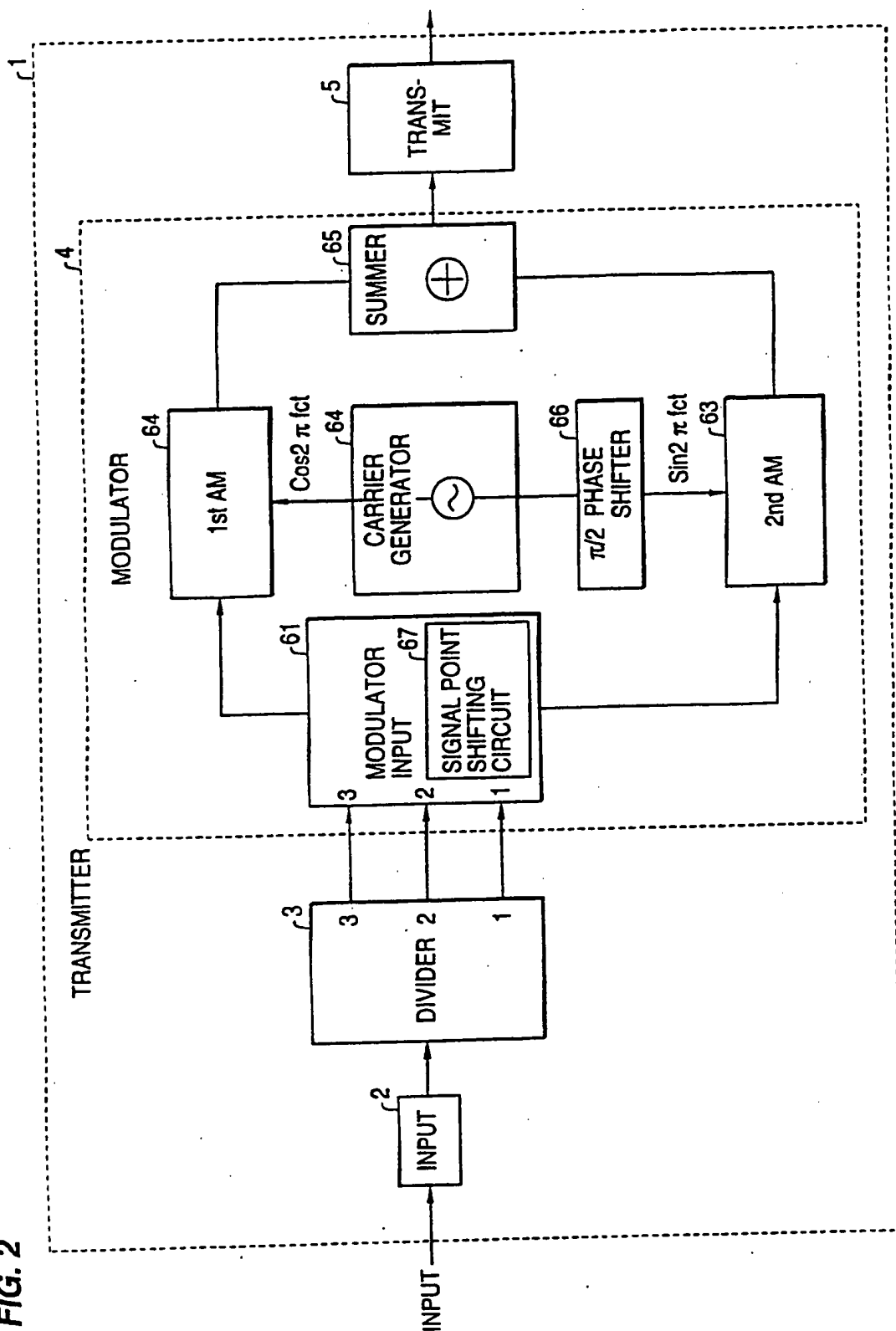


FIG. 4

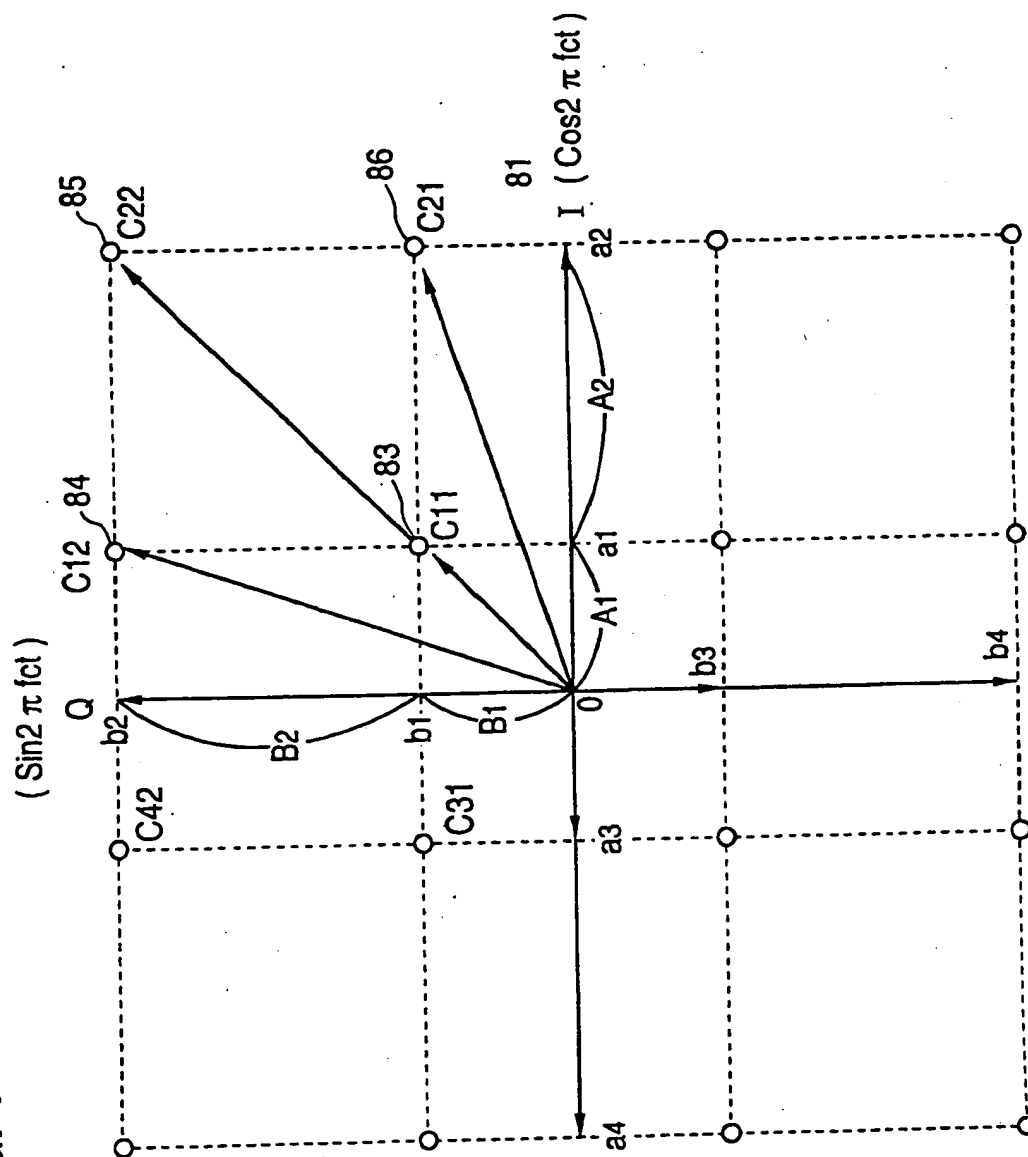


FIG. 5

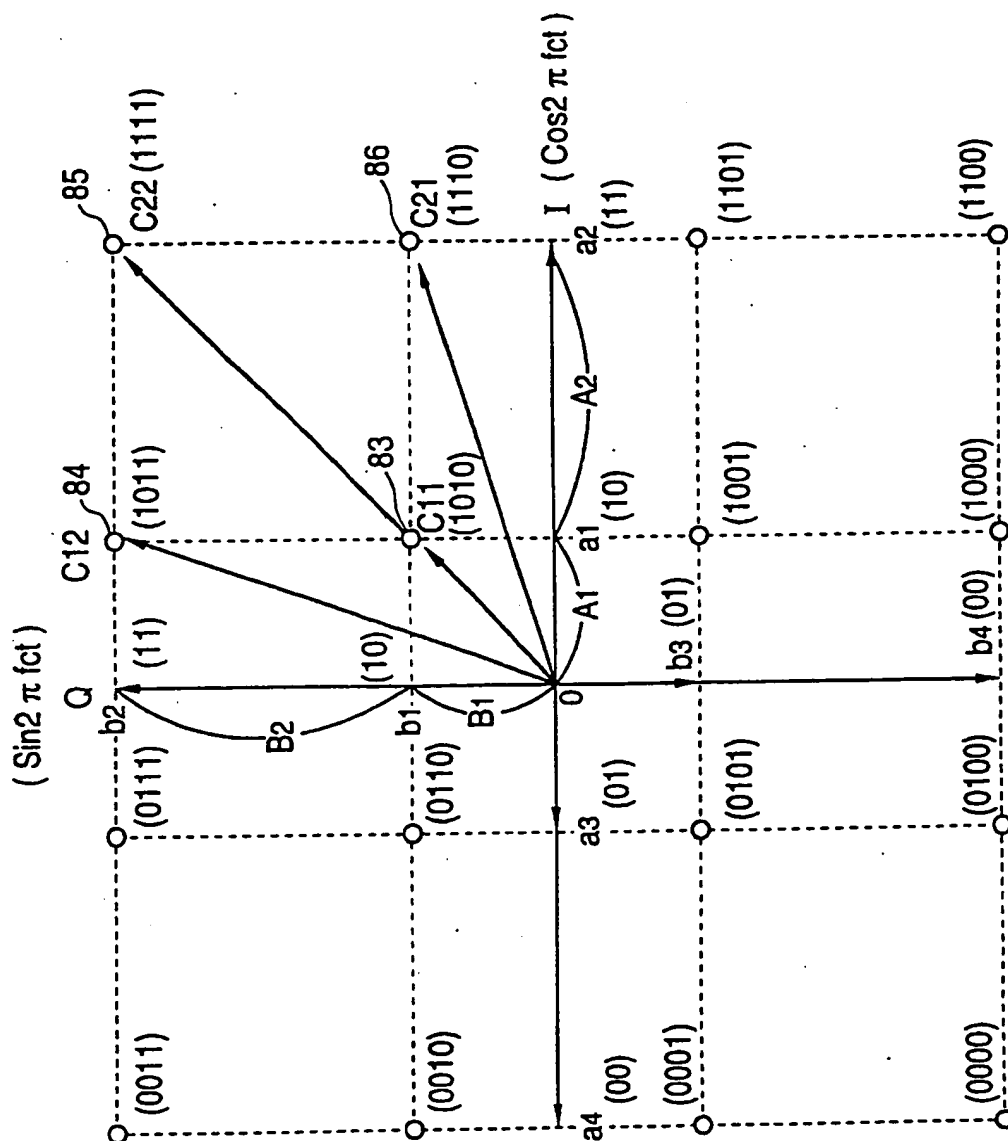


FIG. 6

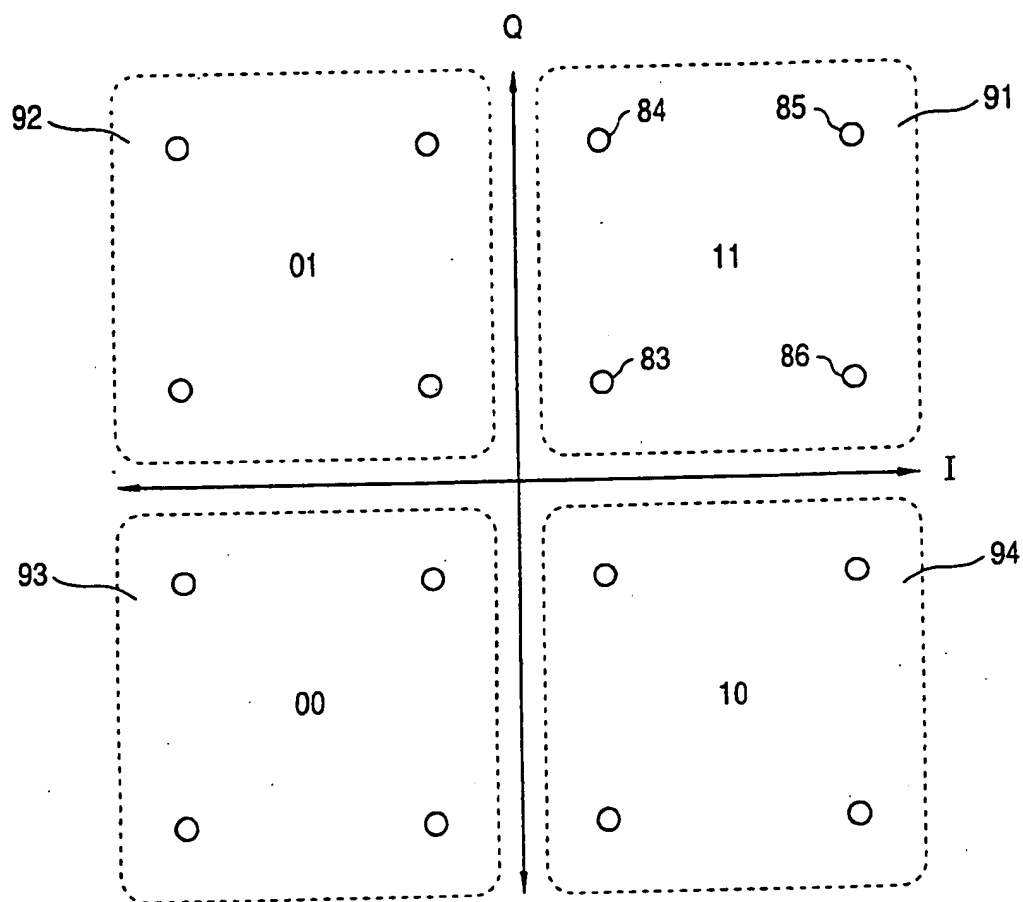


FIG. 7

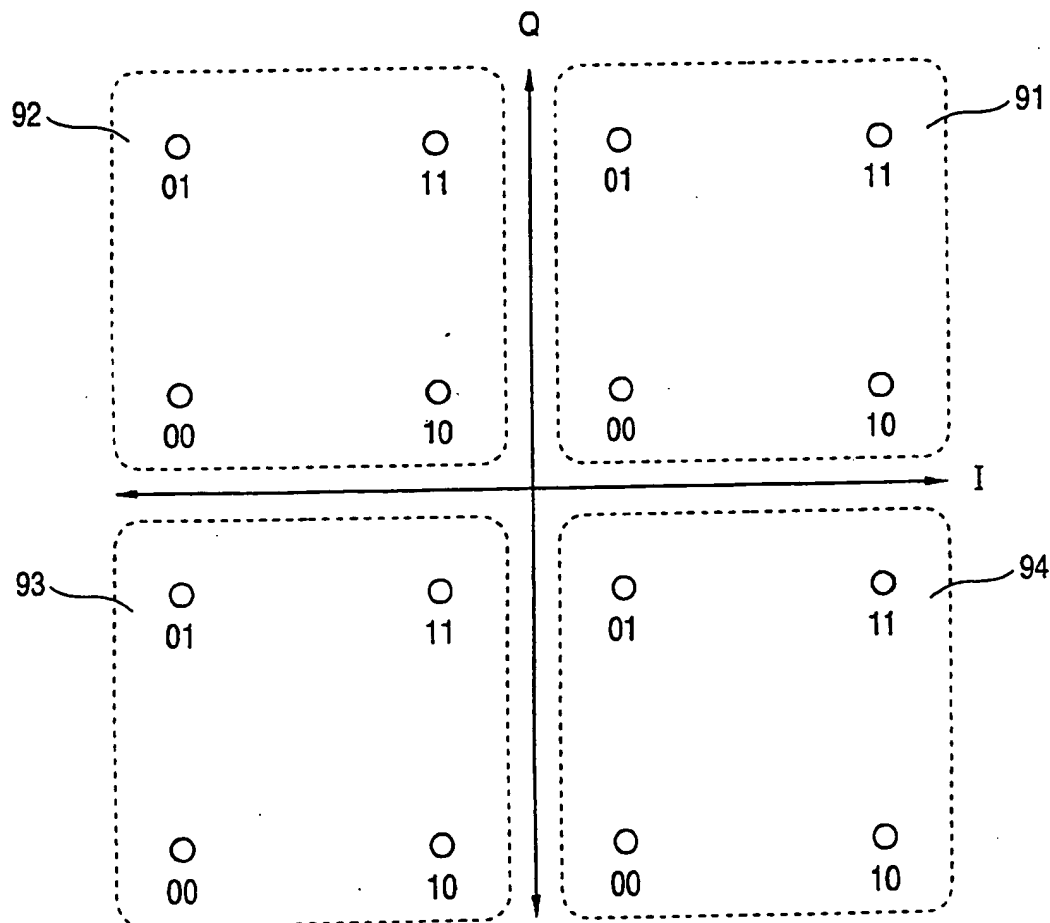


FIG. 8

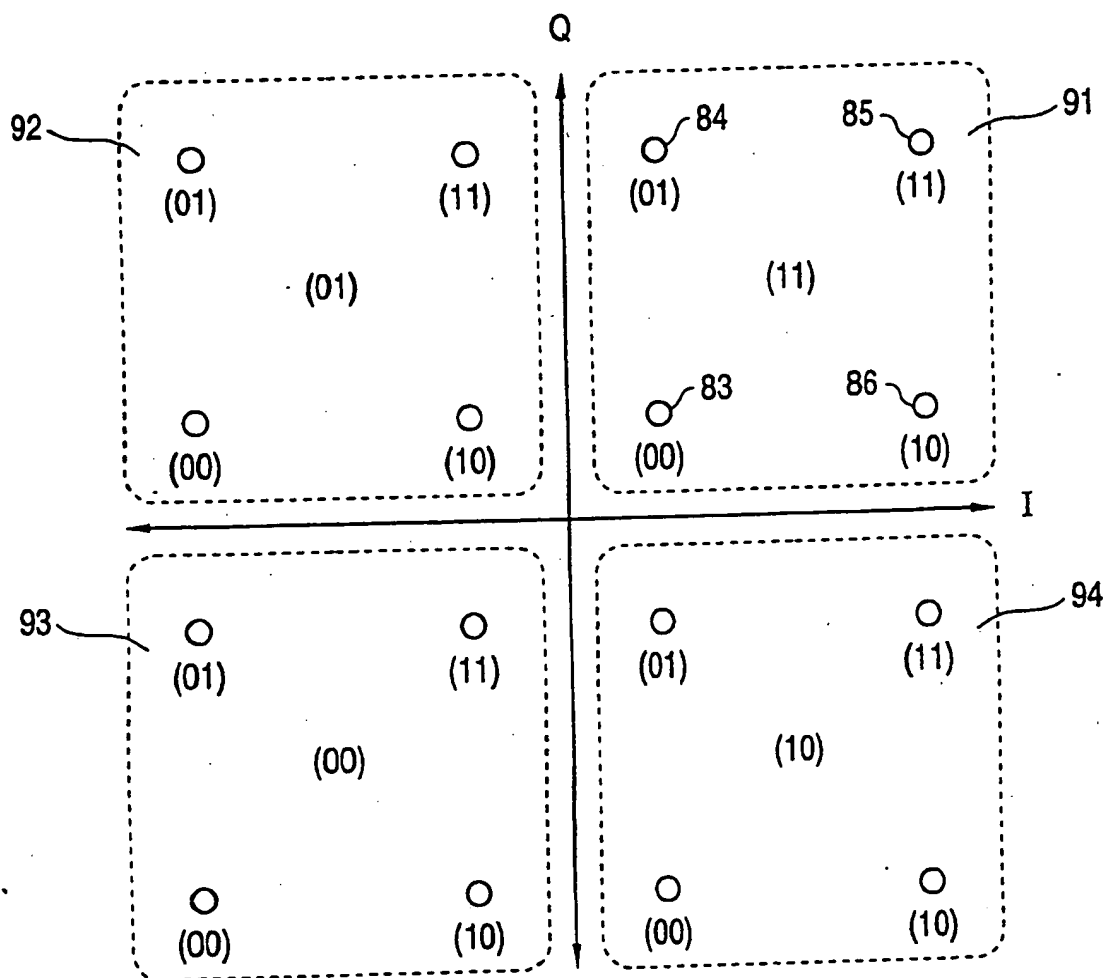


FIG. 9

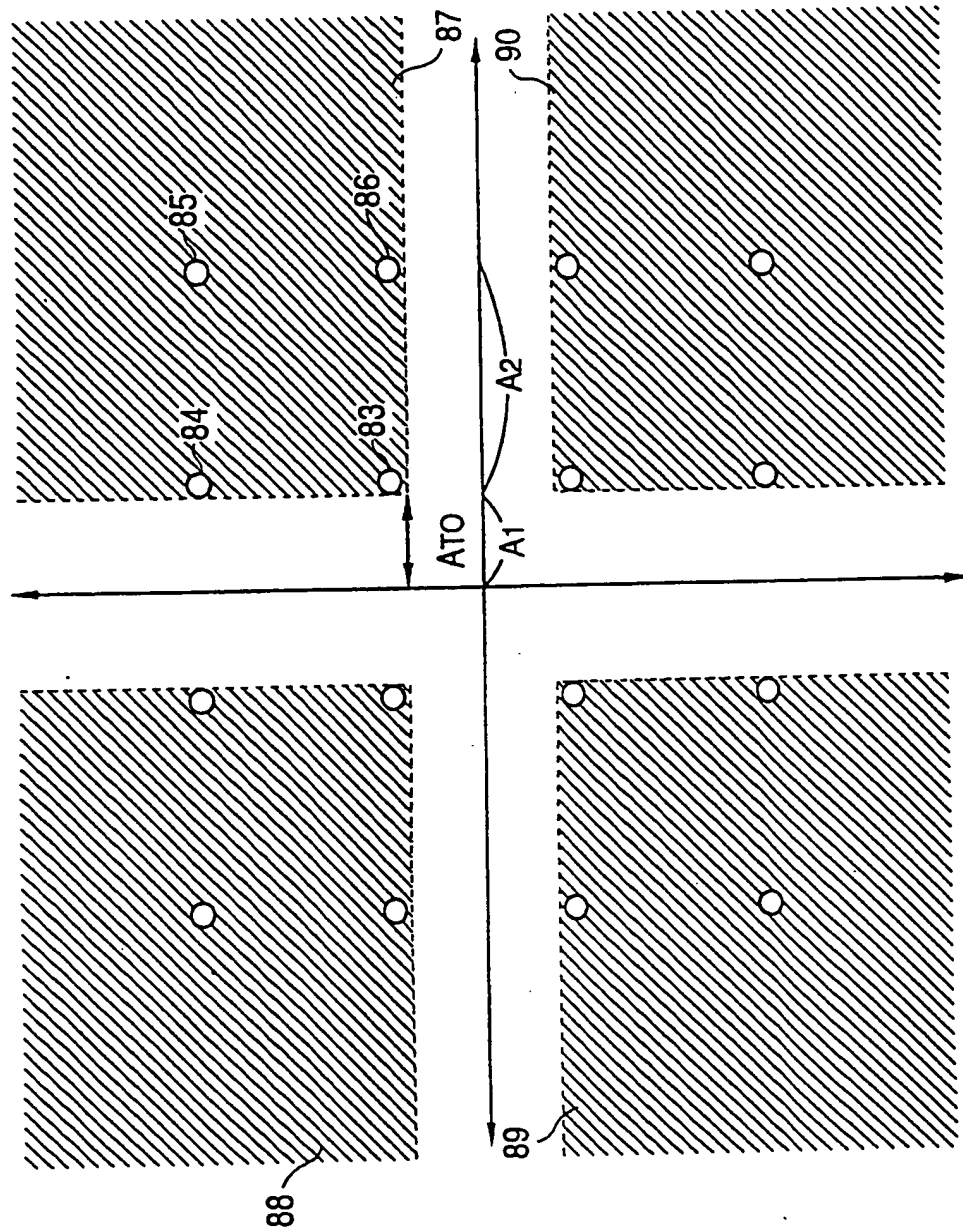


FIG. 10

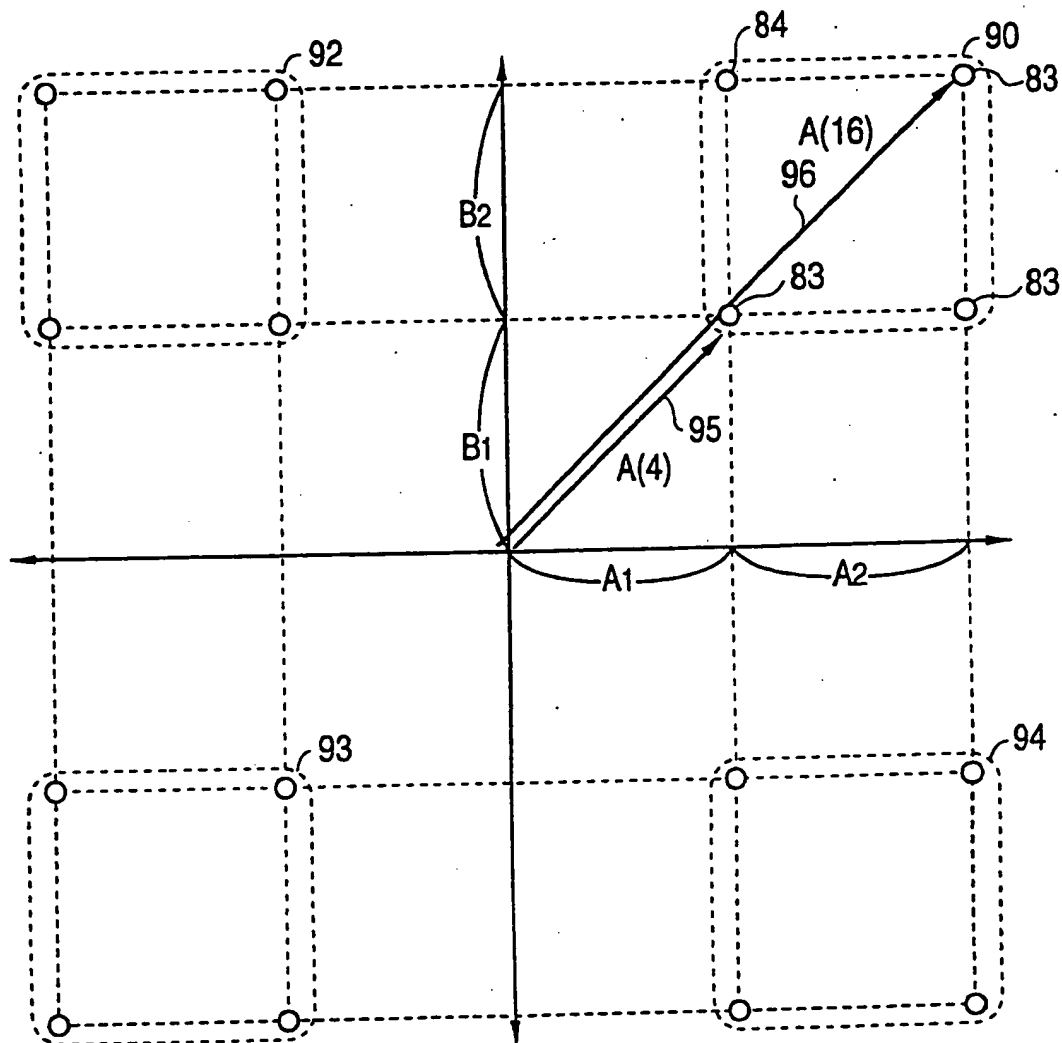
[illegible]

FIG. 11

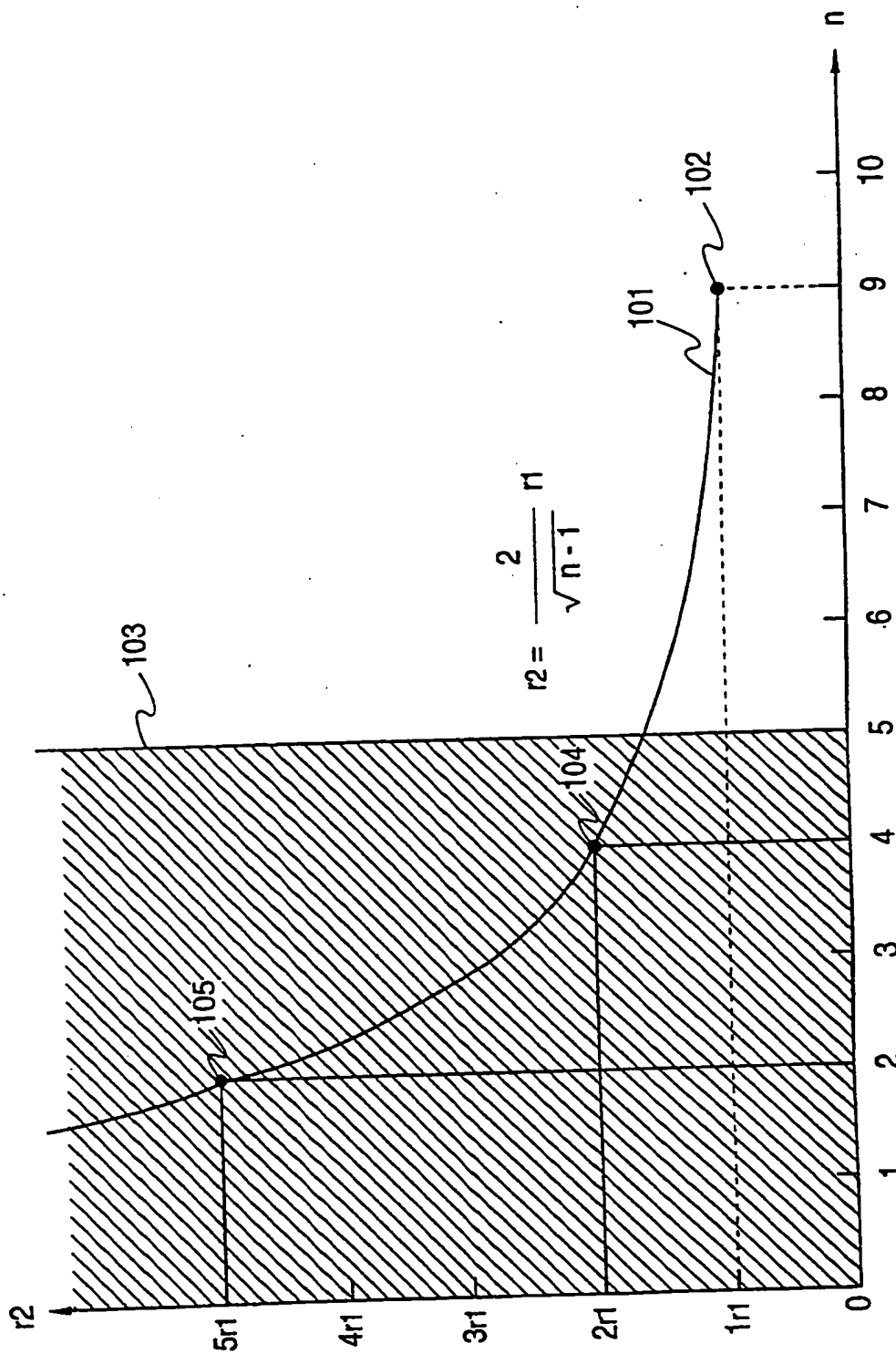


FIG. 12

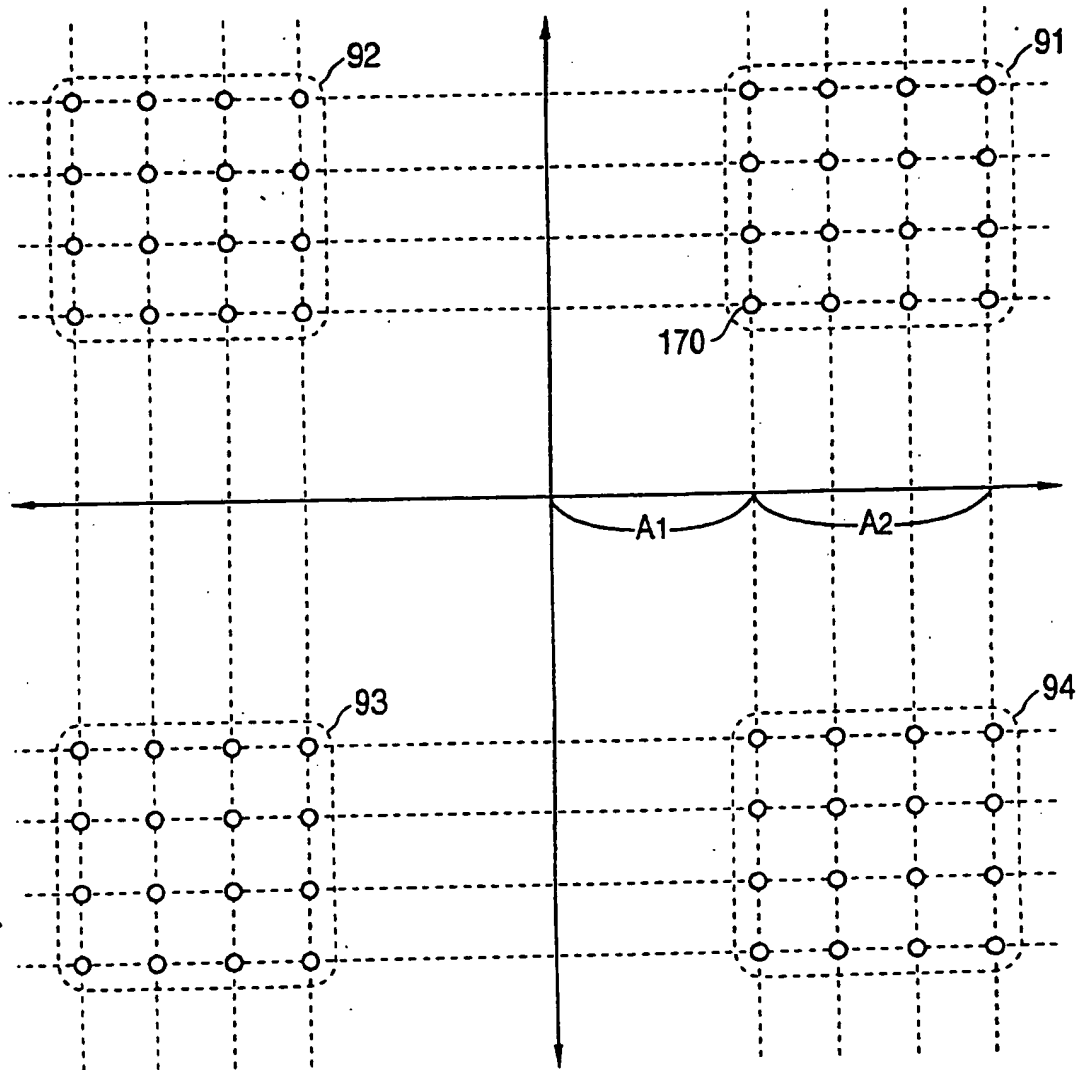


FIG. 13

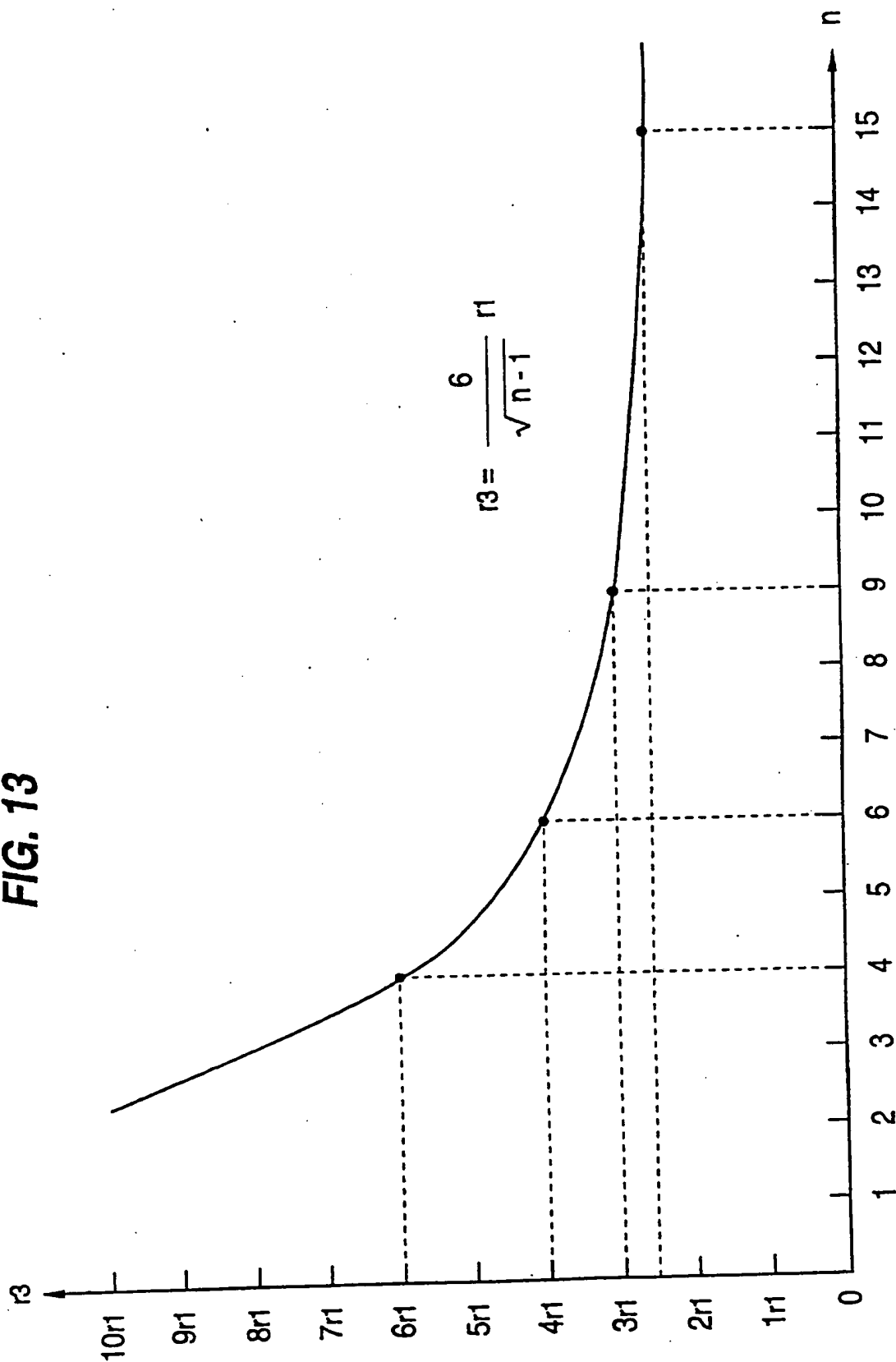


FIG. 14

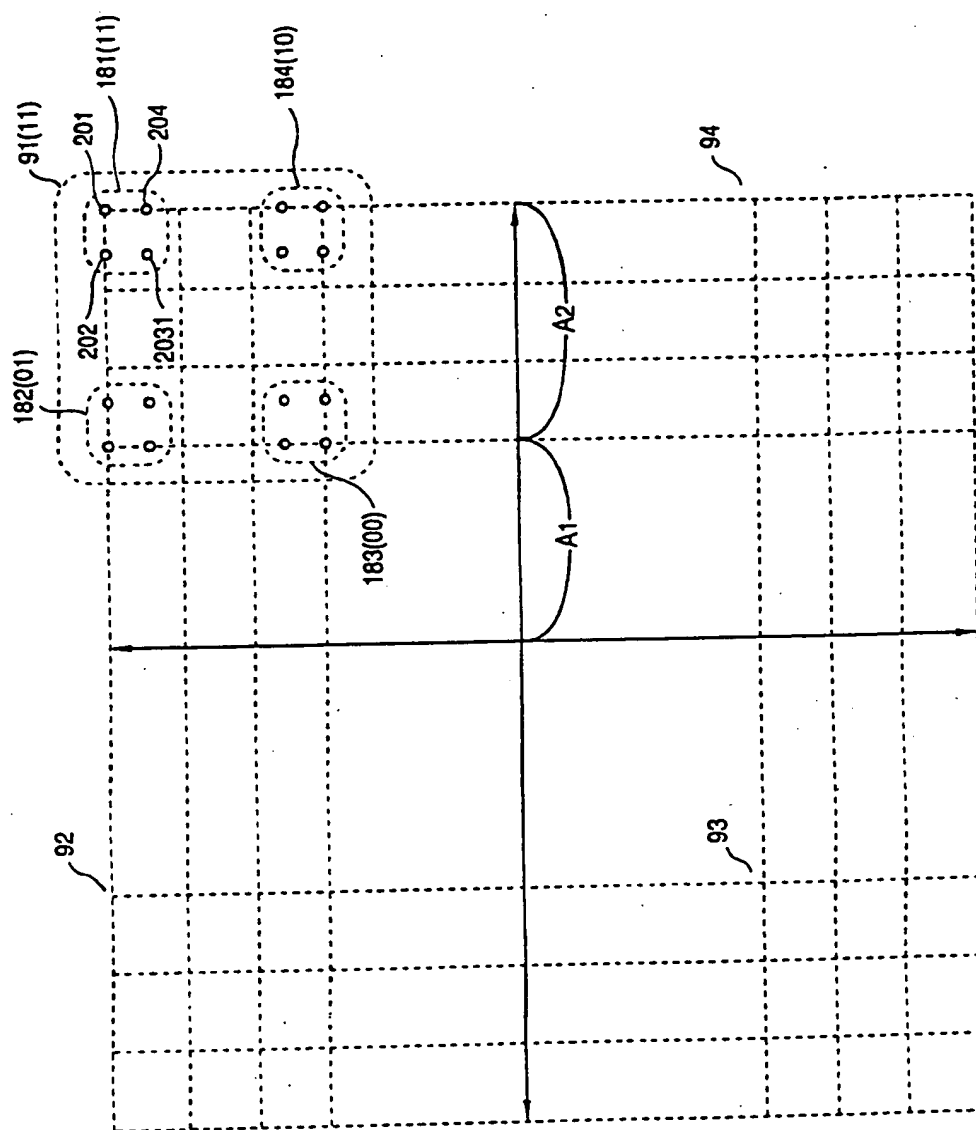


FIG. 15

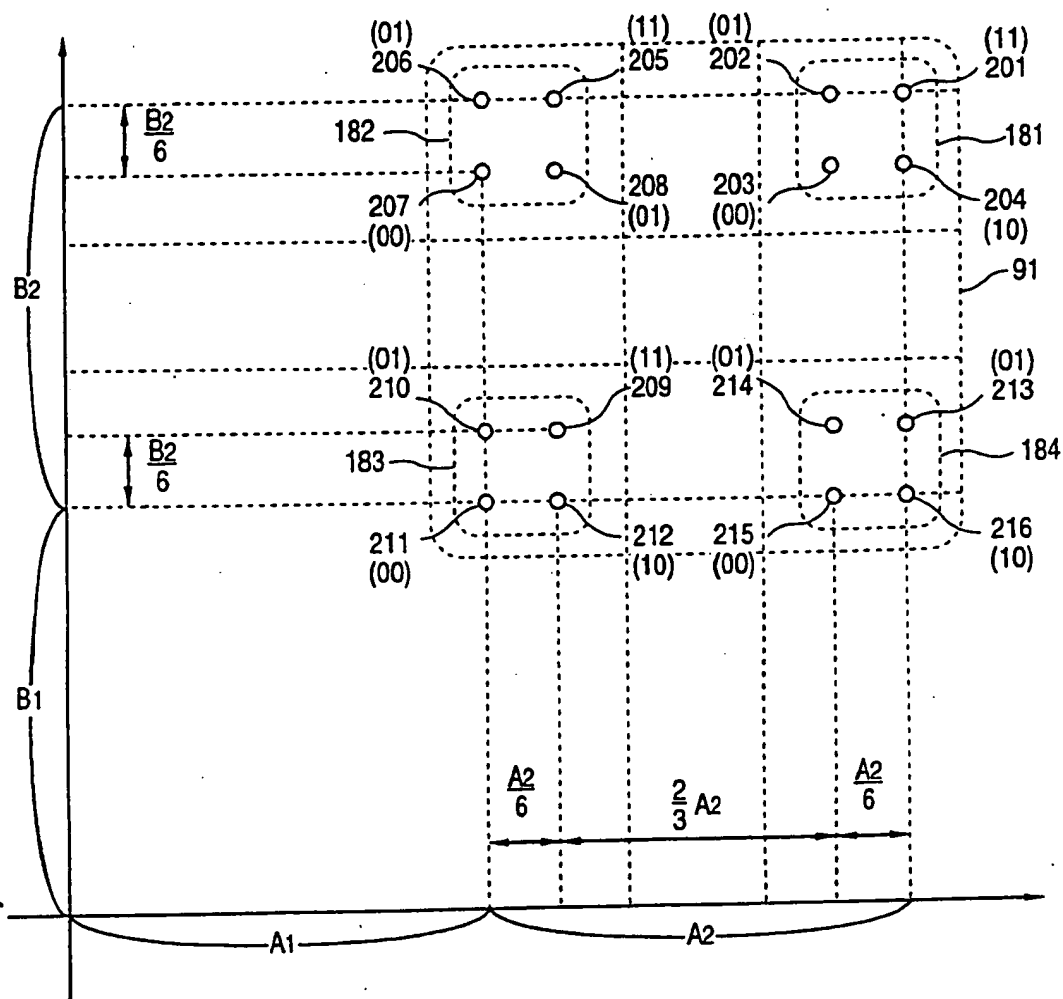


FIG. 16

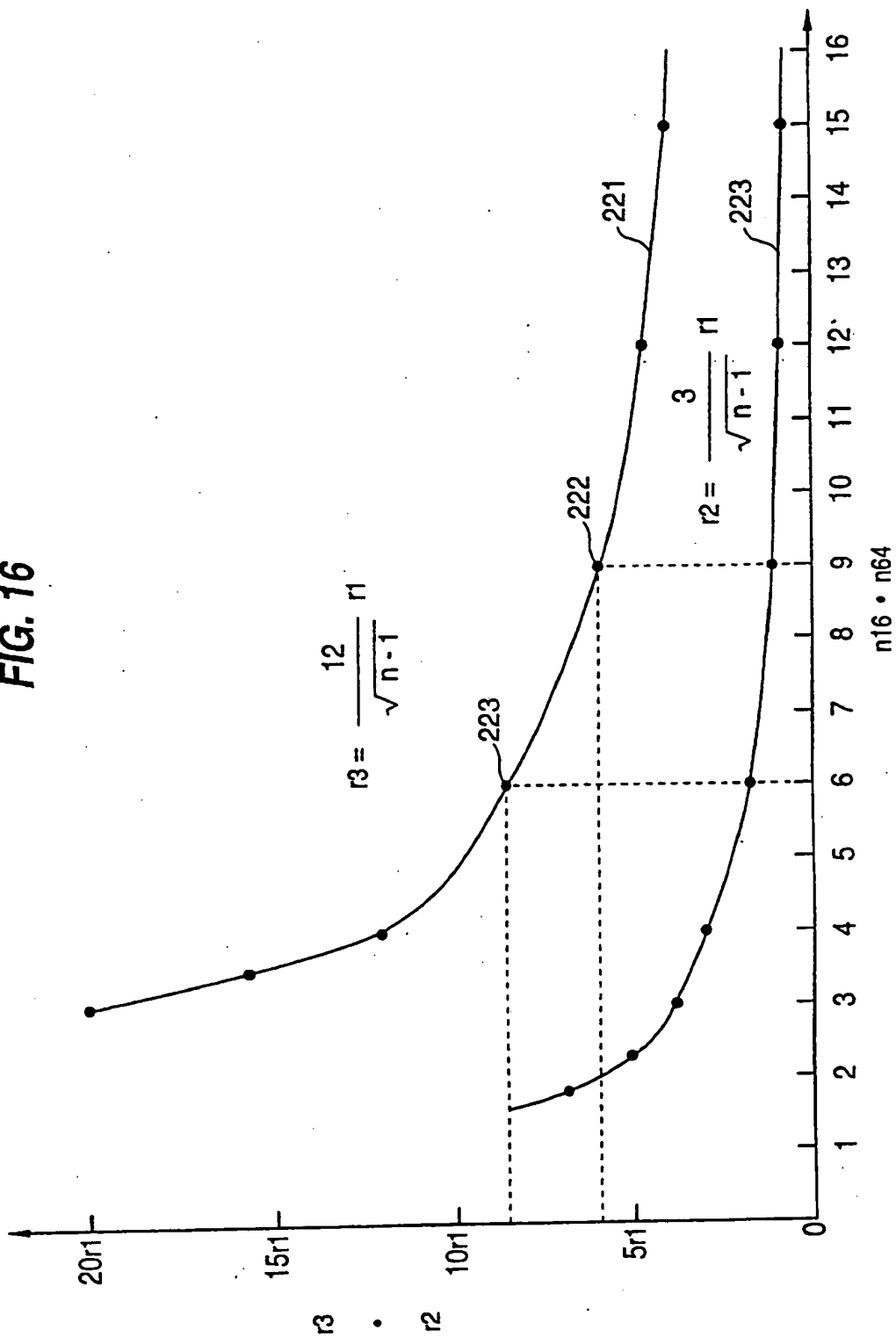


FIG. 17

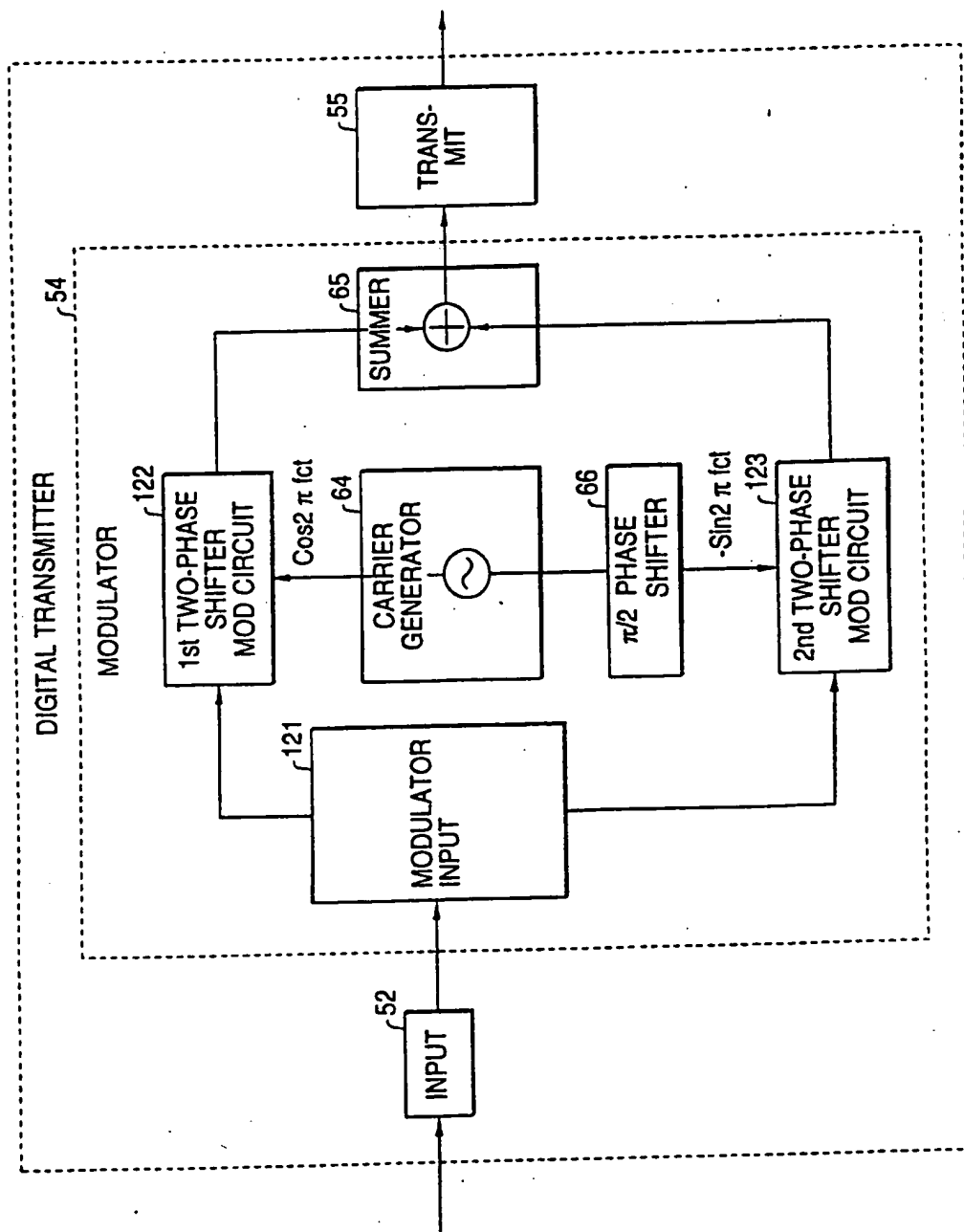
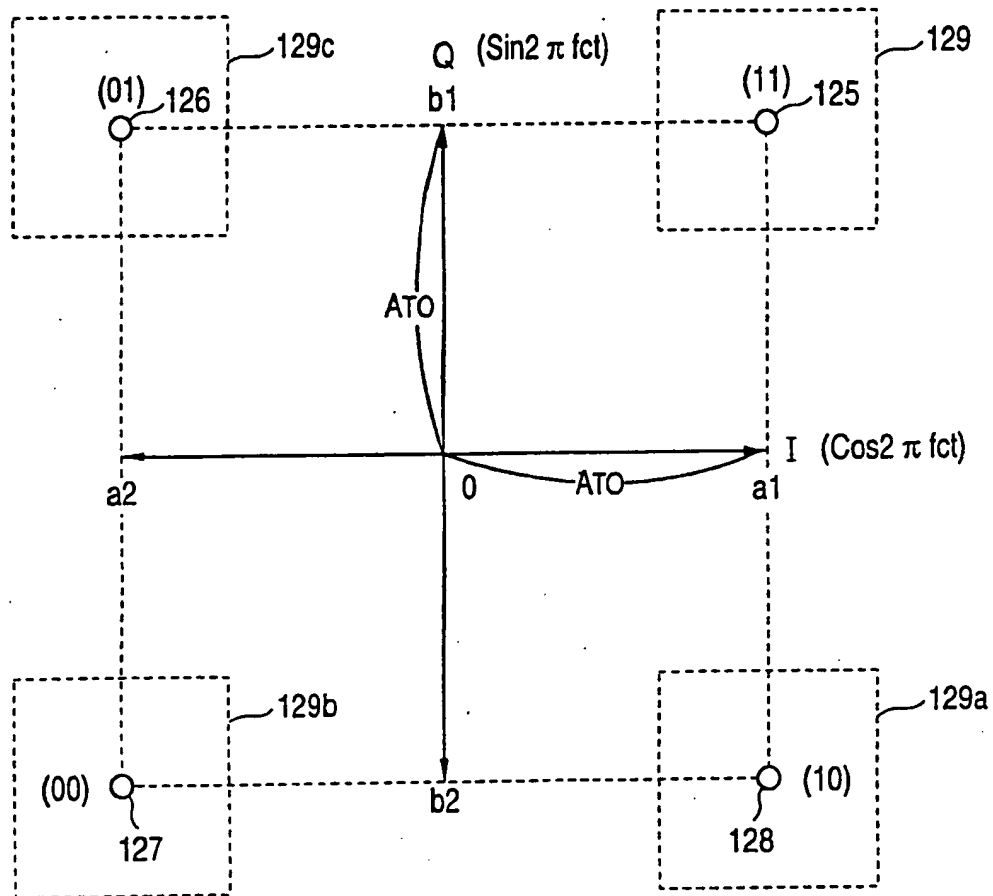


FIG. 18



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FIG. 19

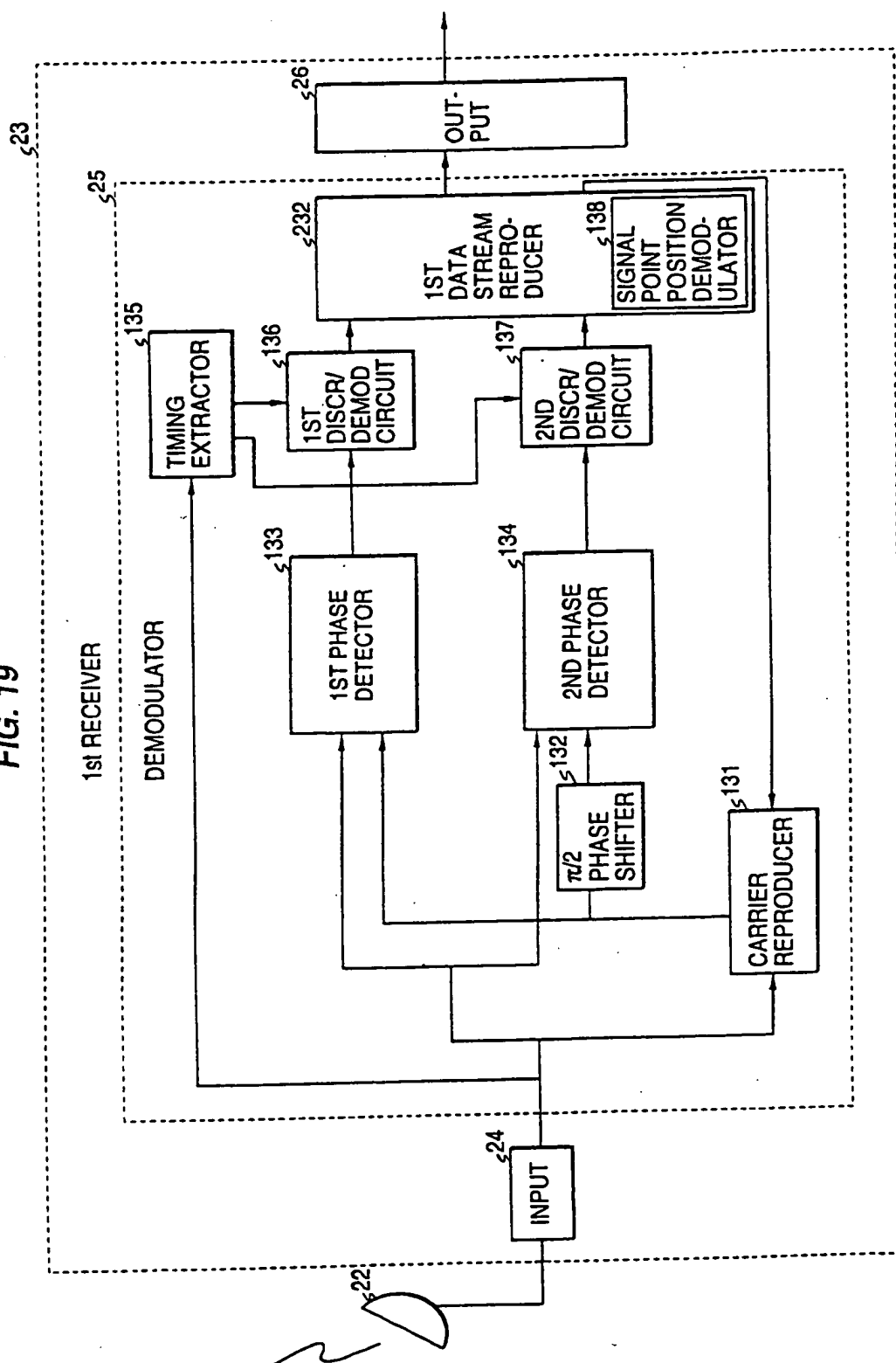
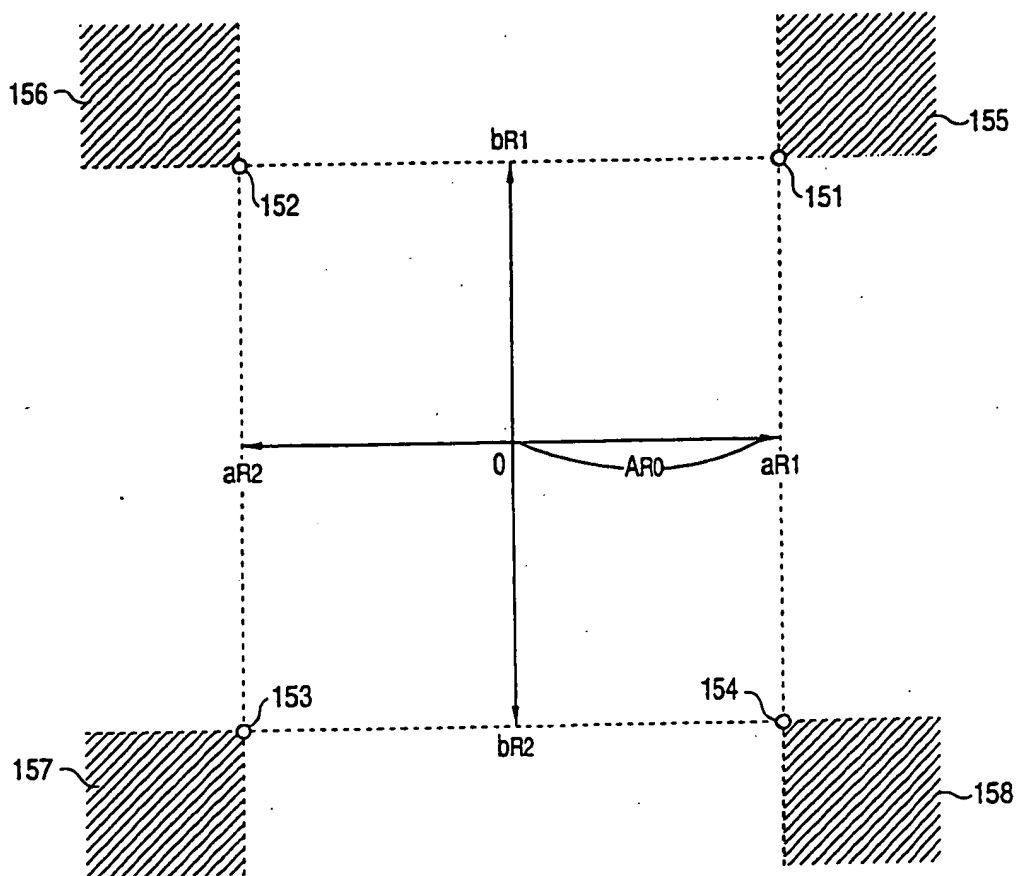


FIG. 20



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FIG. 21

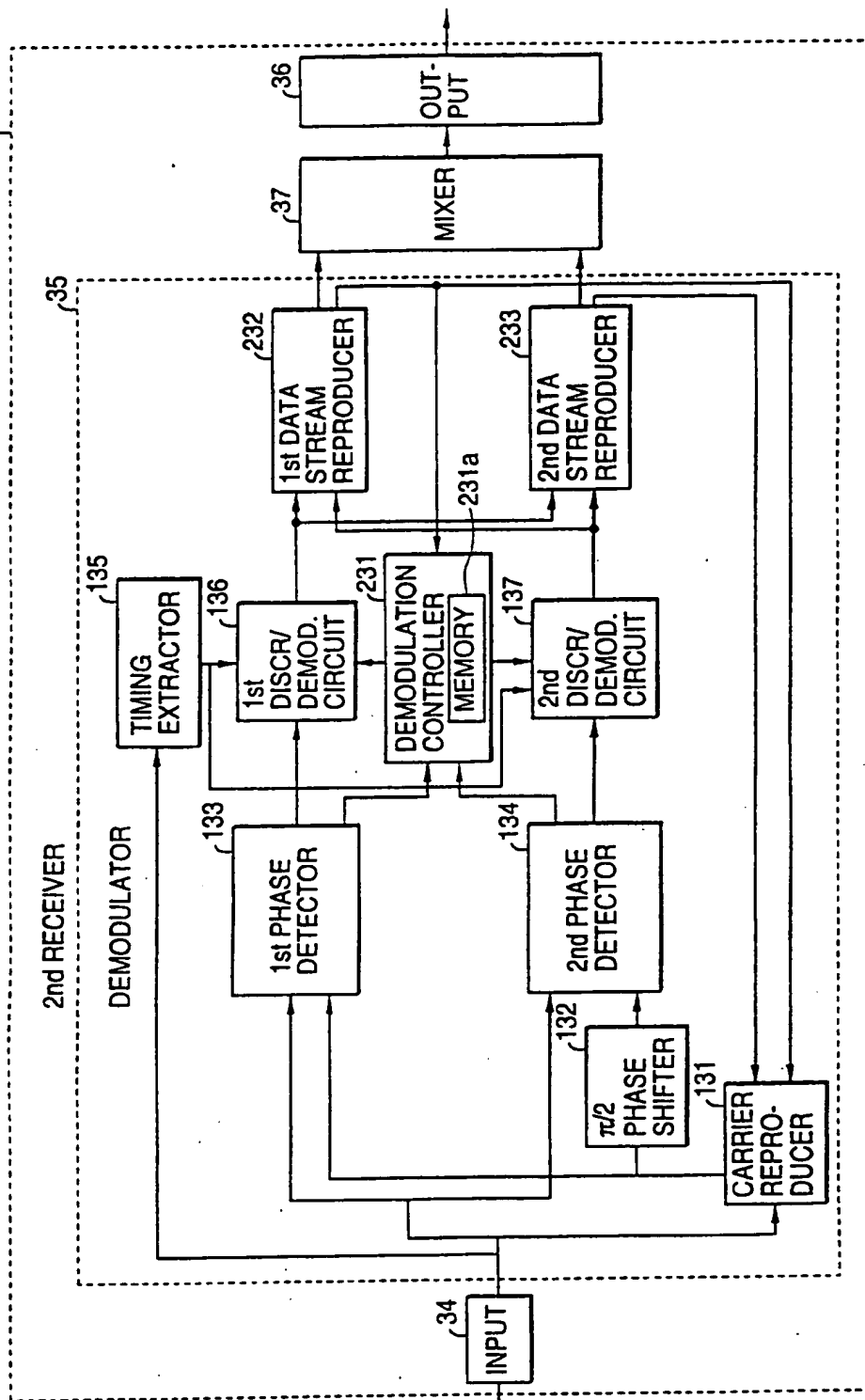
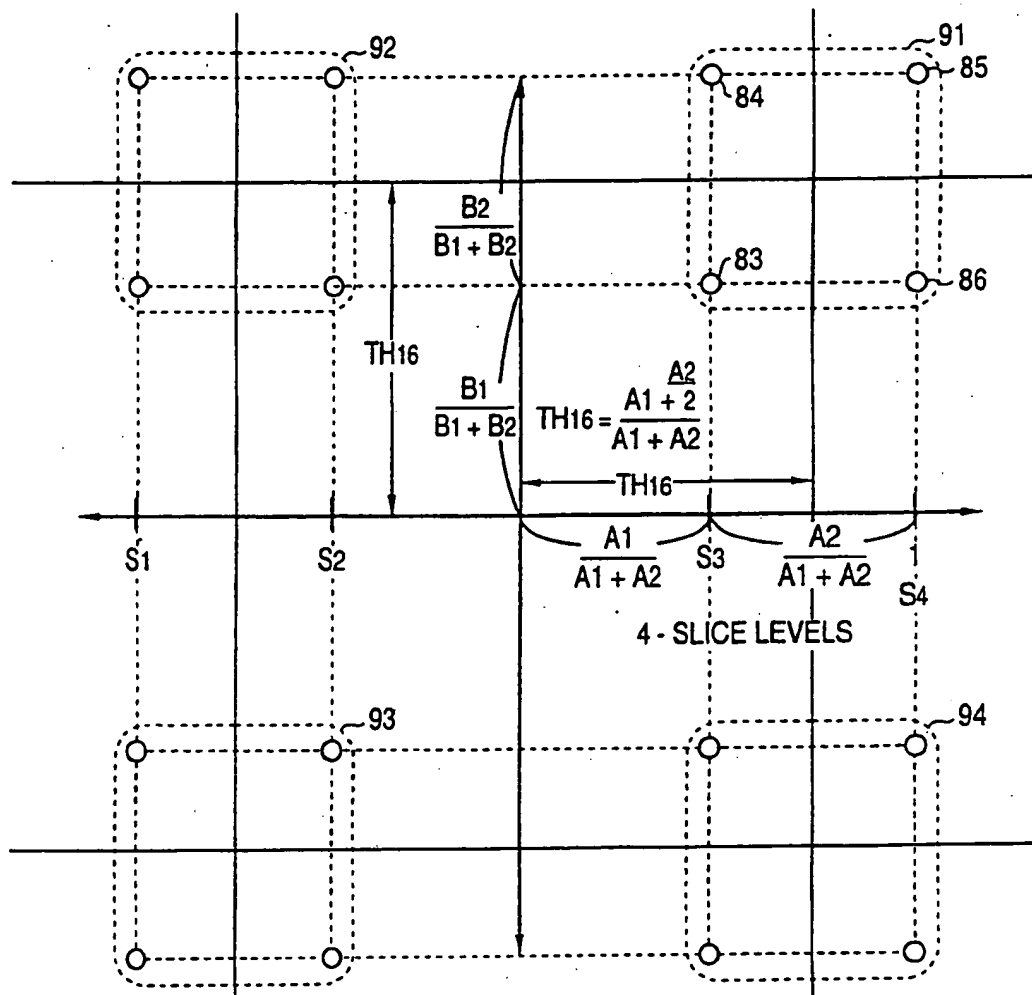


FIG. 22



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FIG. 23

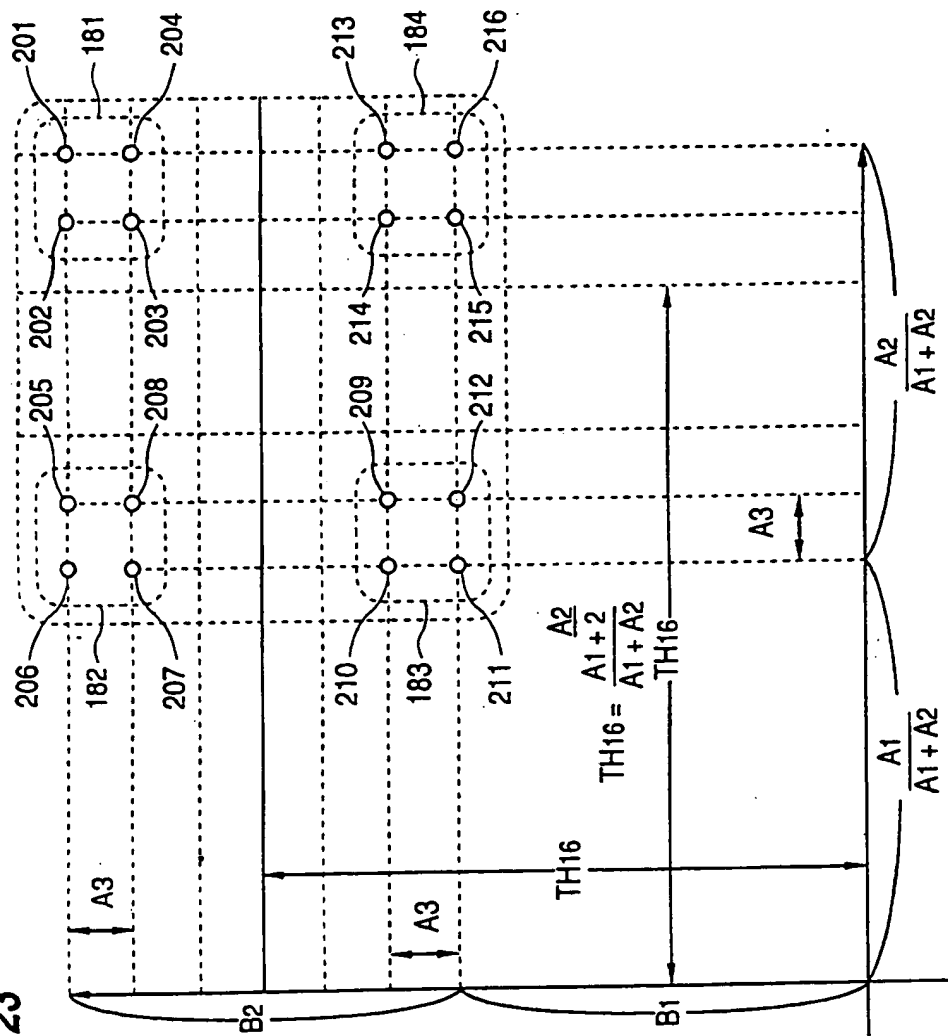


FIG. 24

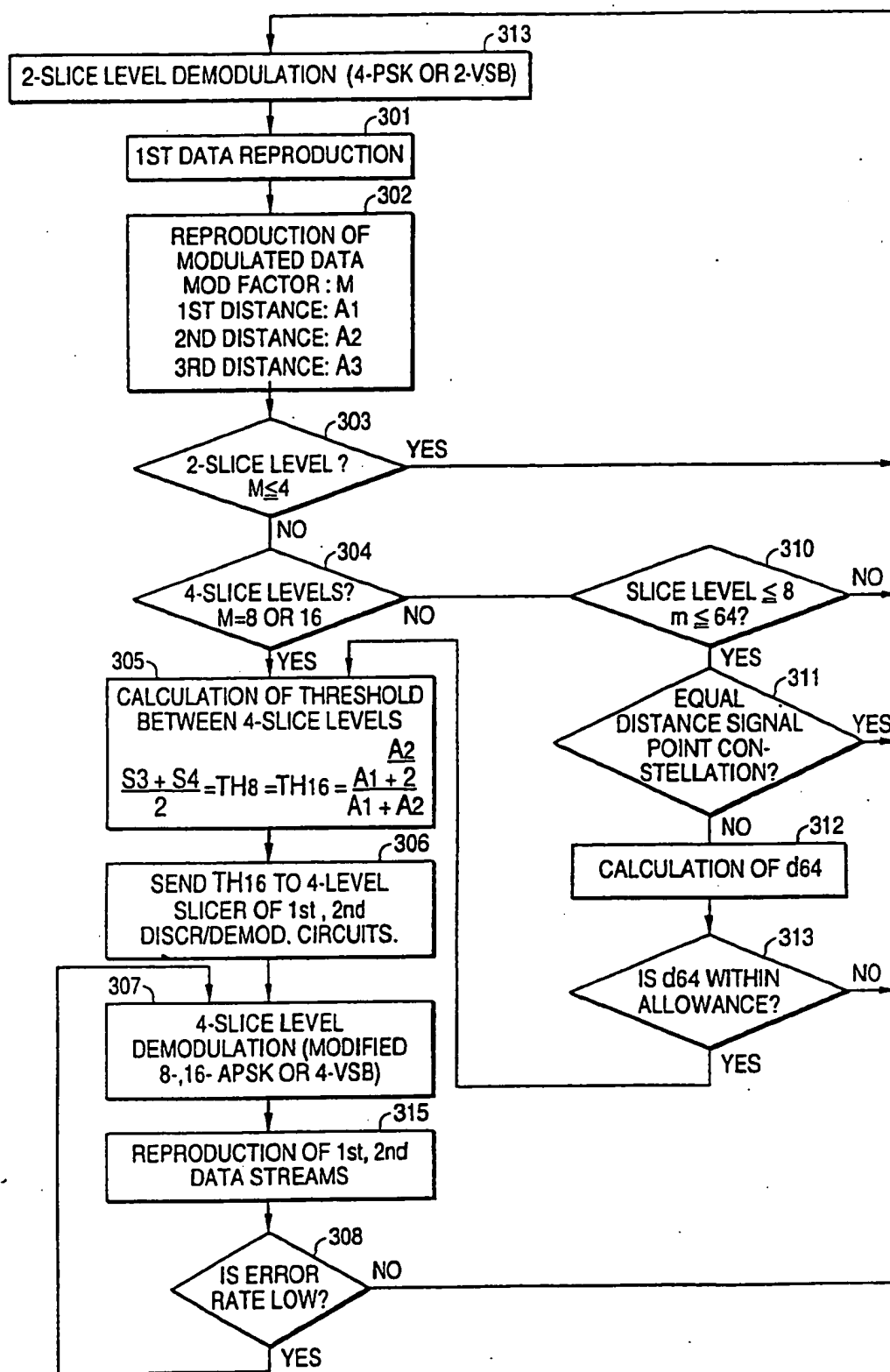


FIG. 25(a)

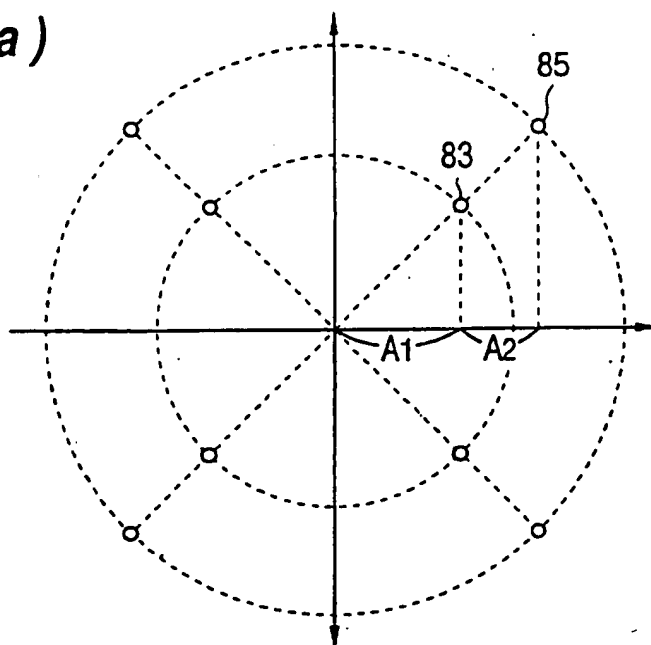
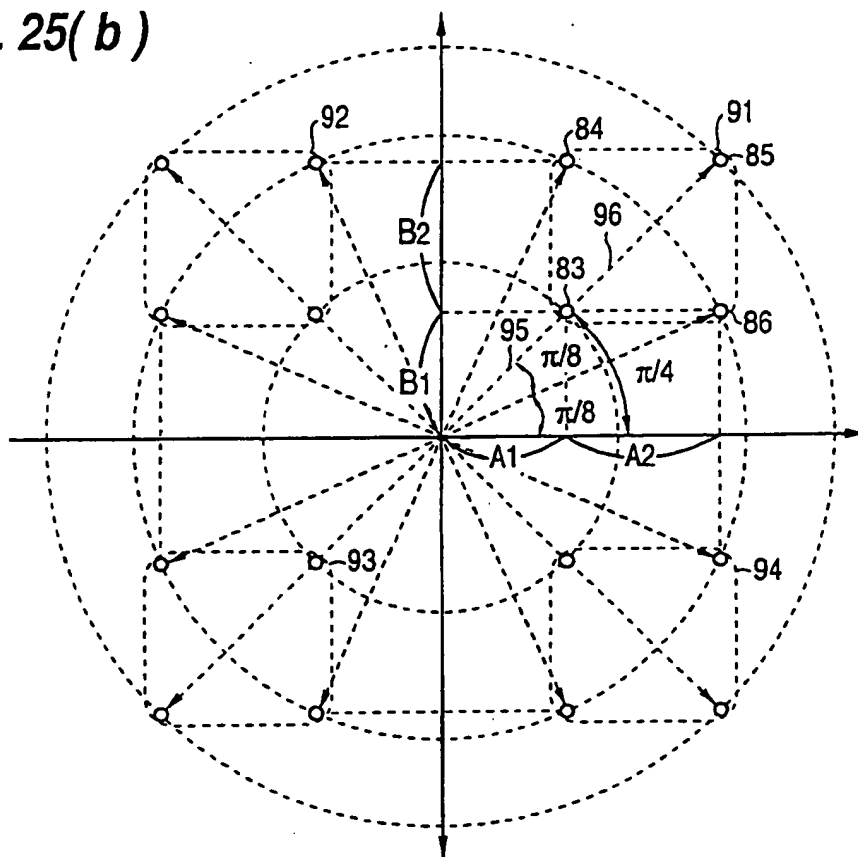
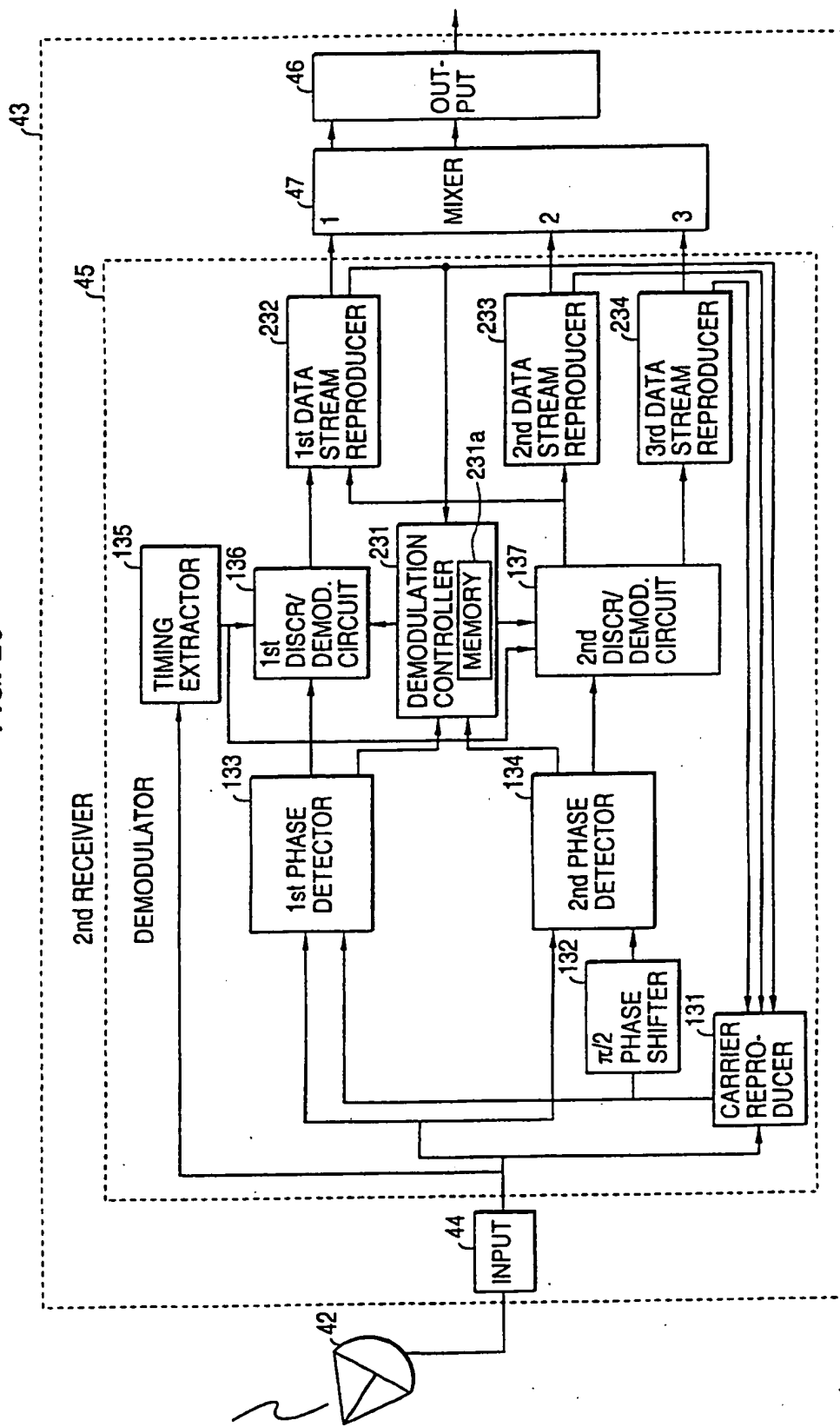


FIG. 25(b)



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FIG. 26



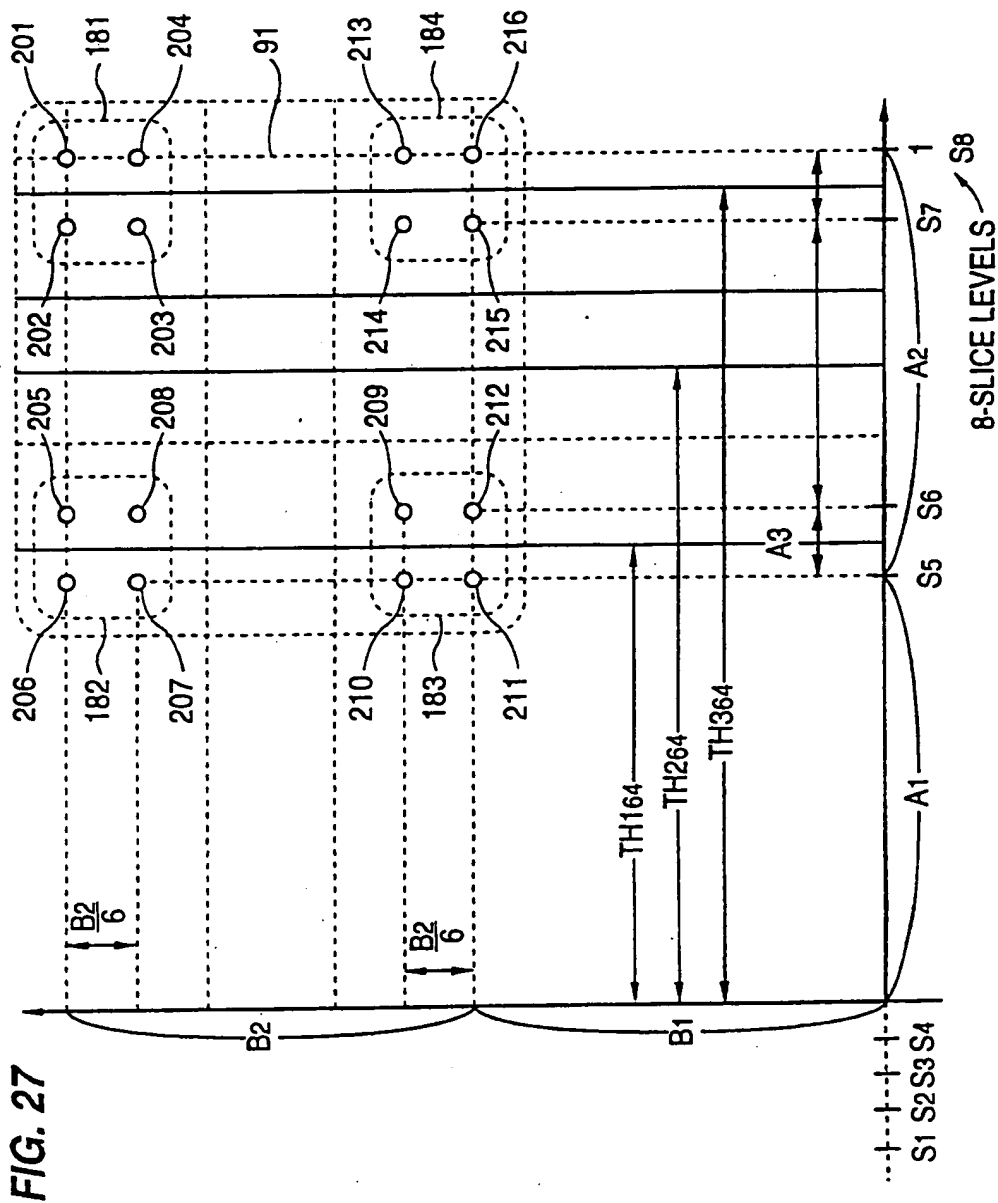


FIG. 28

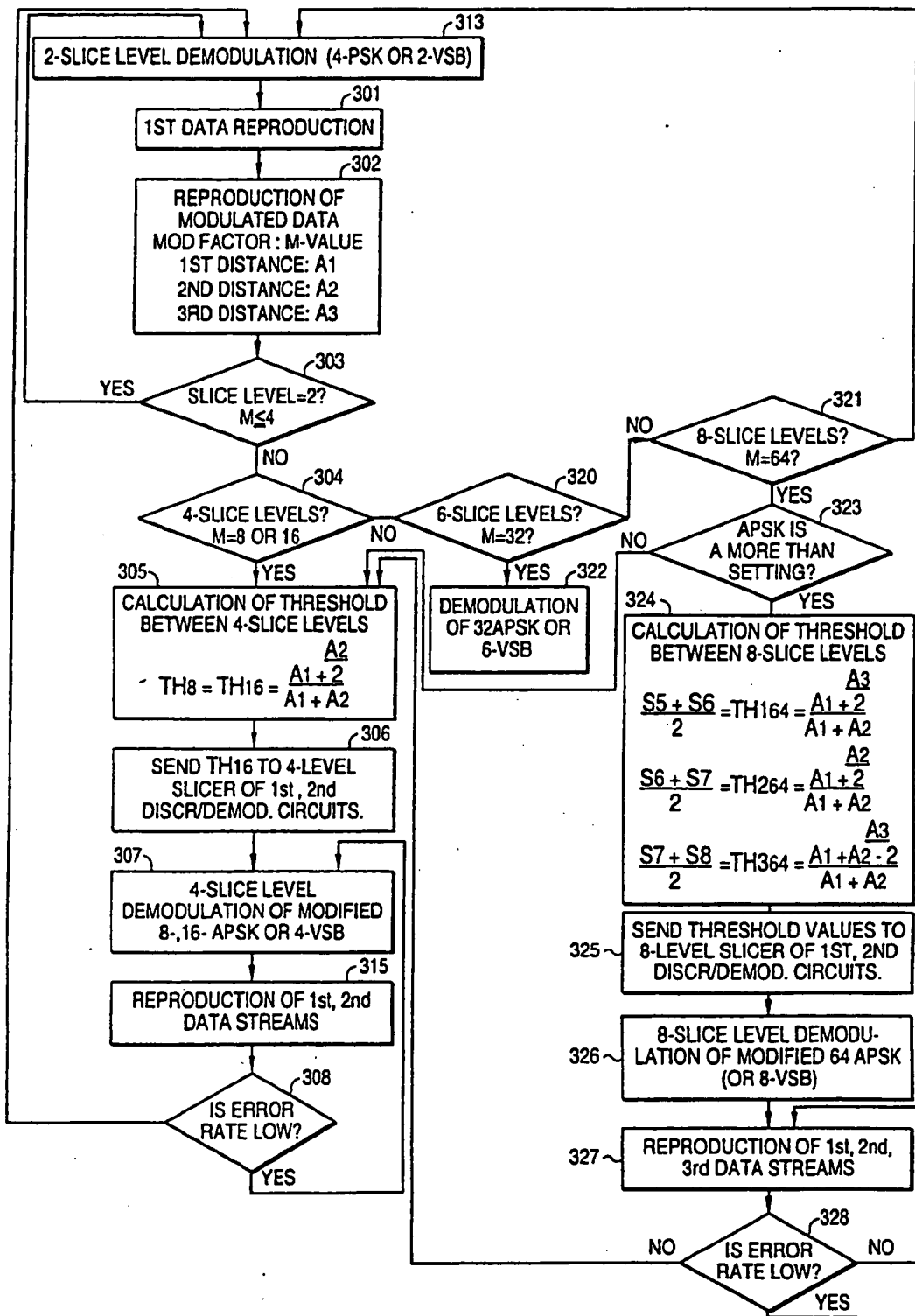


FIG. 29

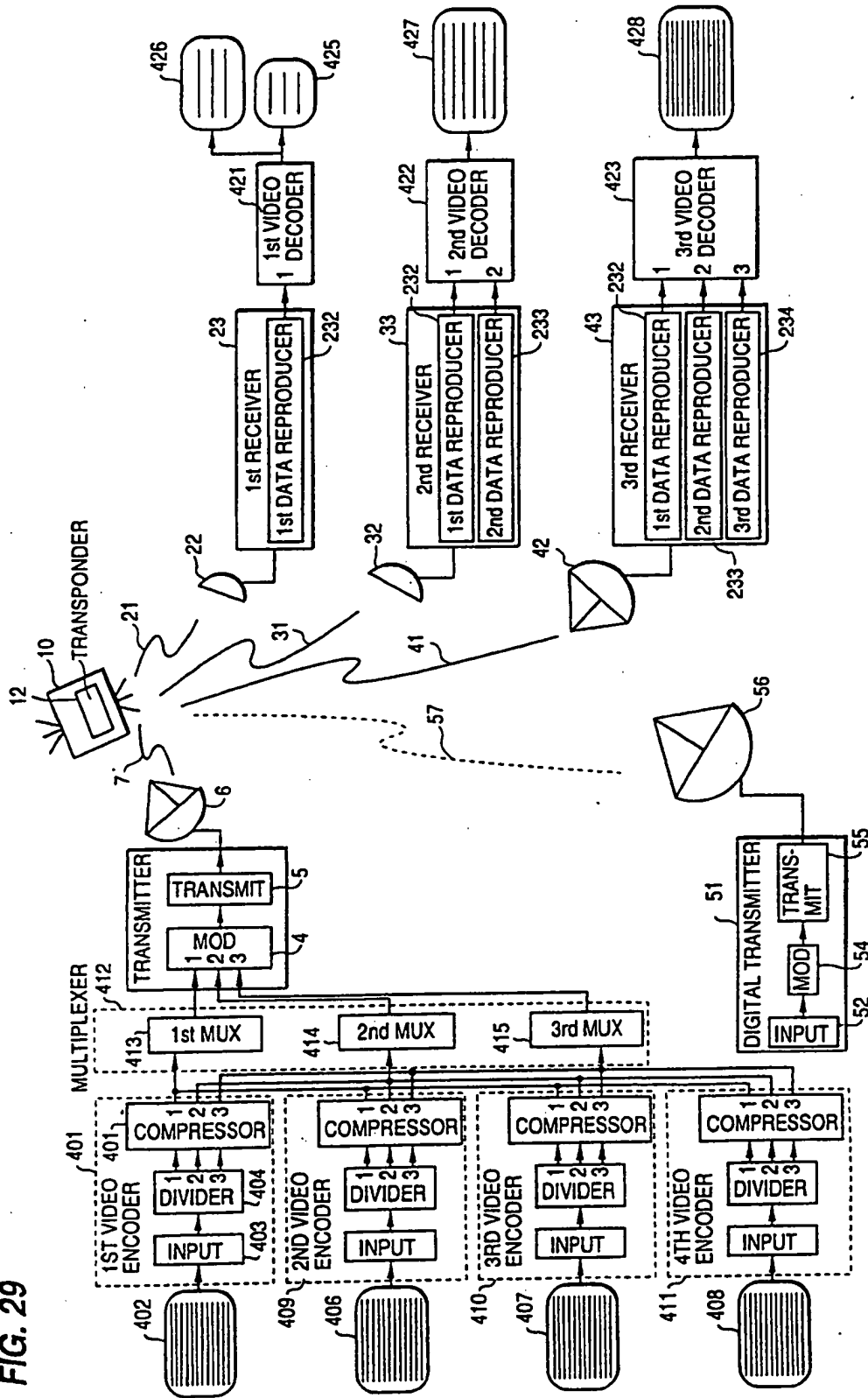
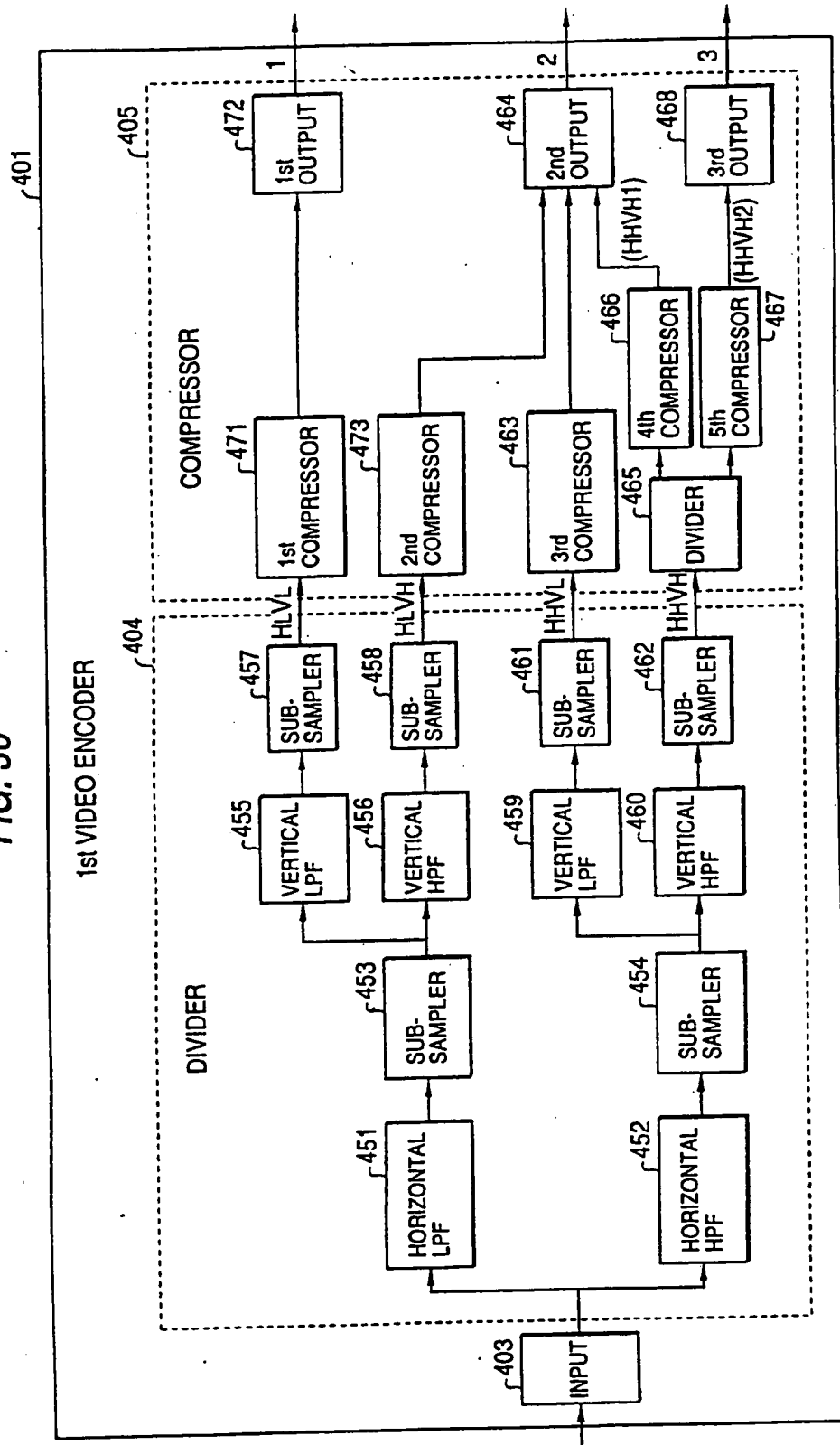
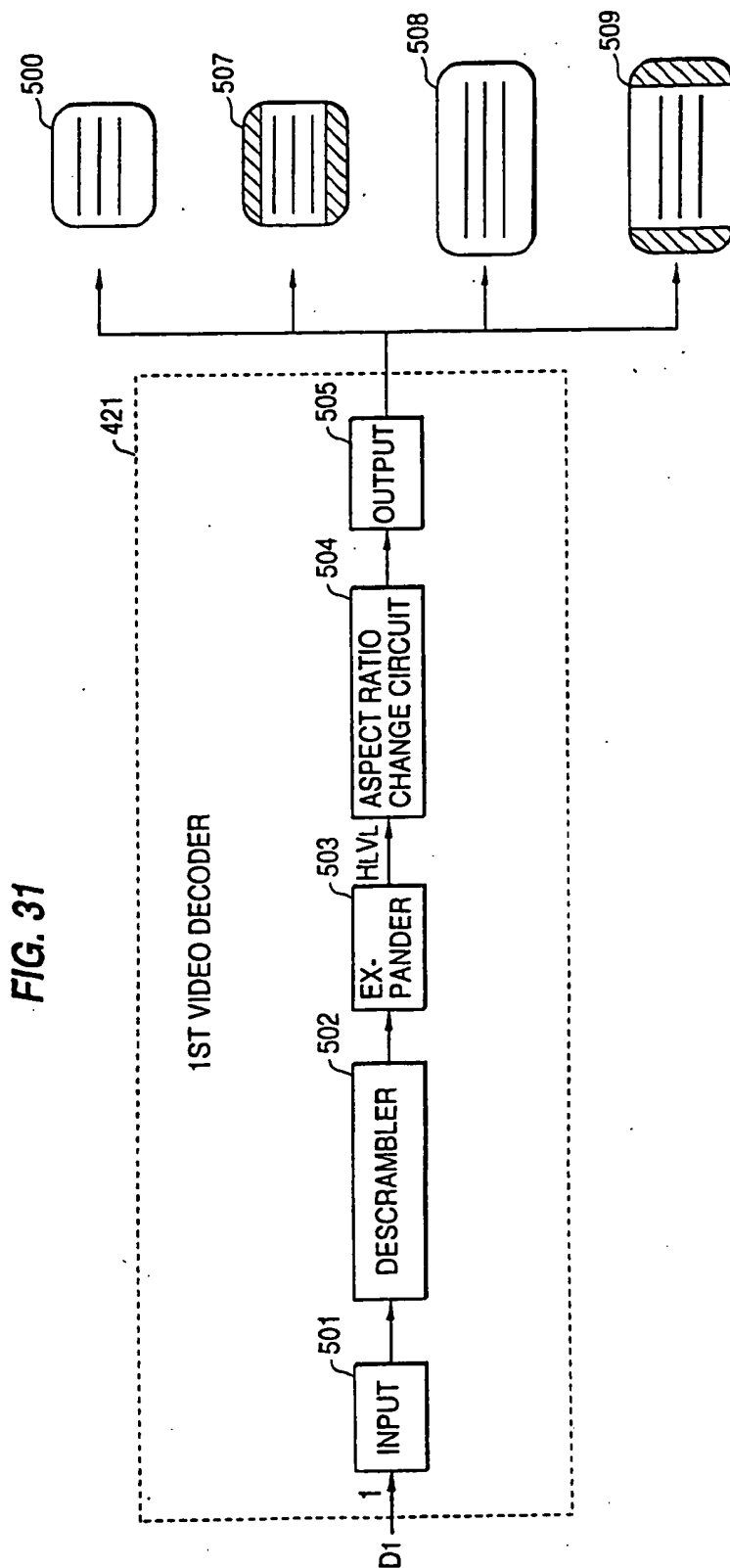


FIG. 30





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[illegible]

FIG. 32

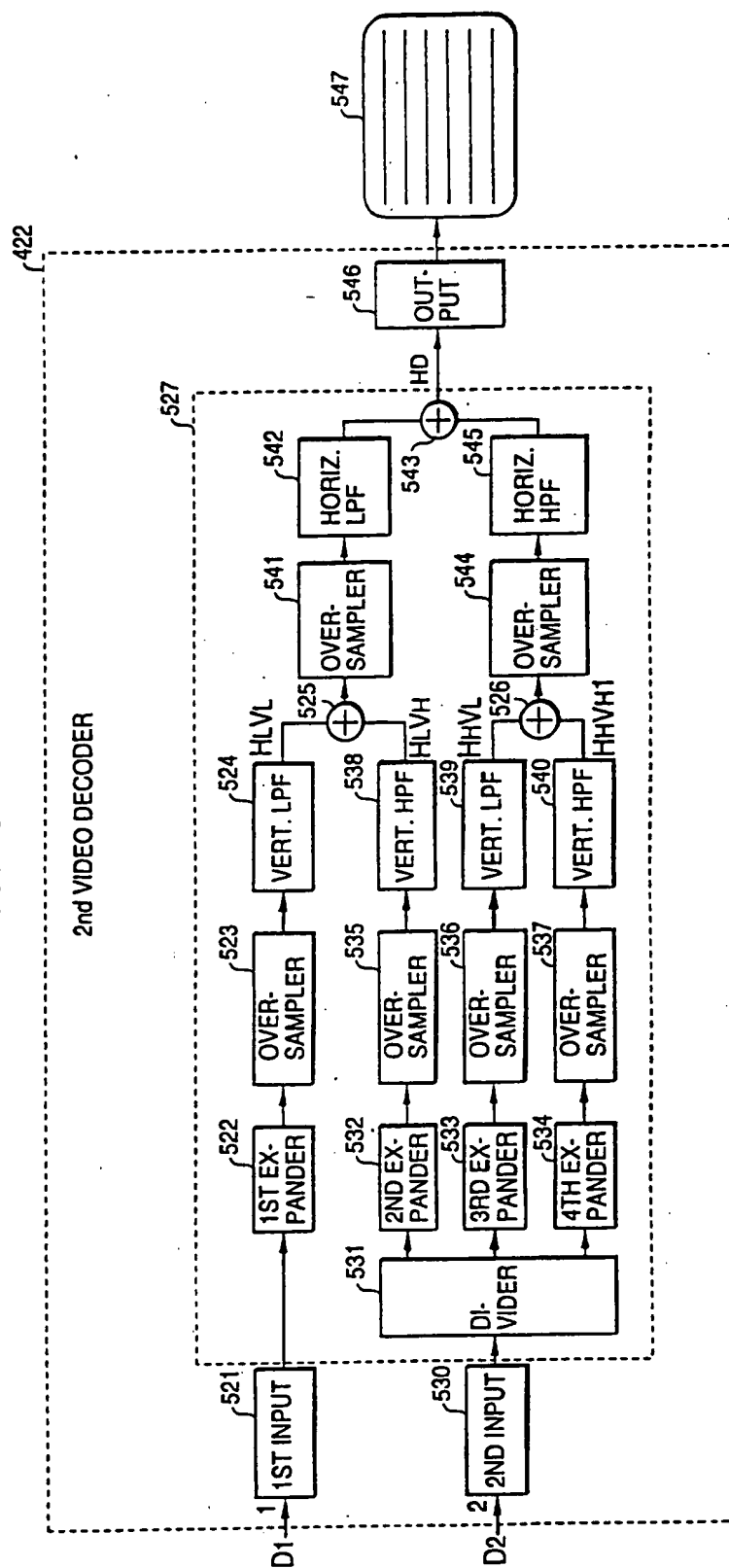


FIG. 33

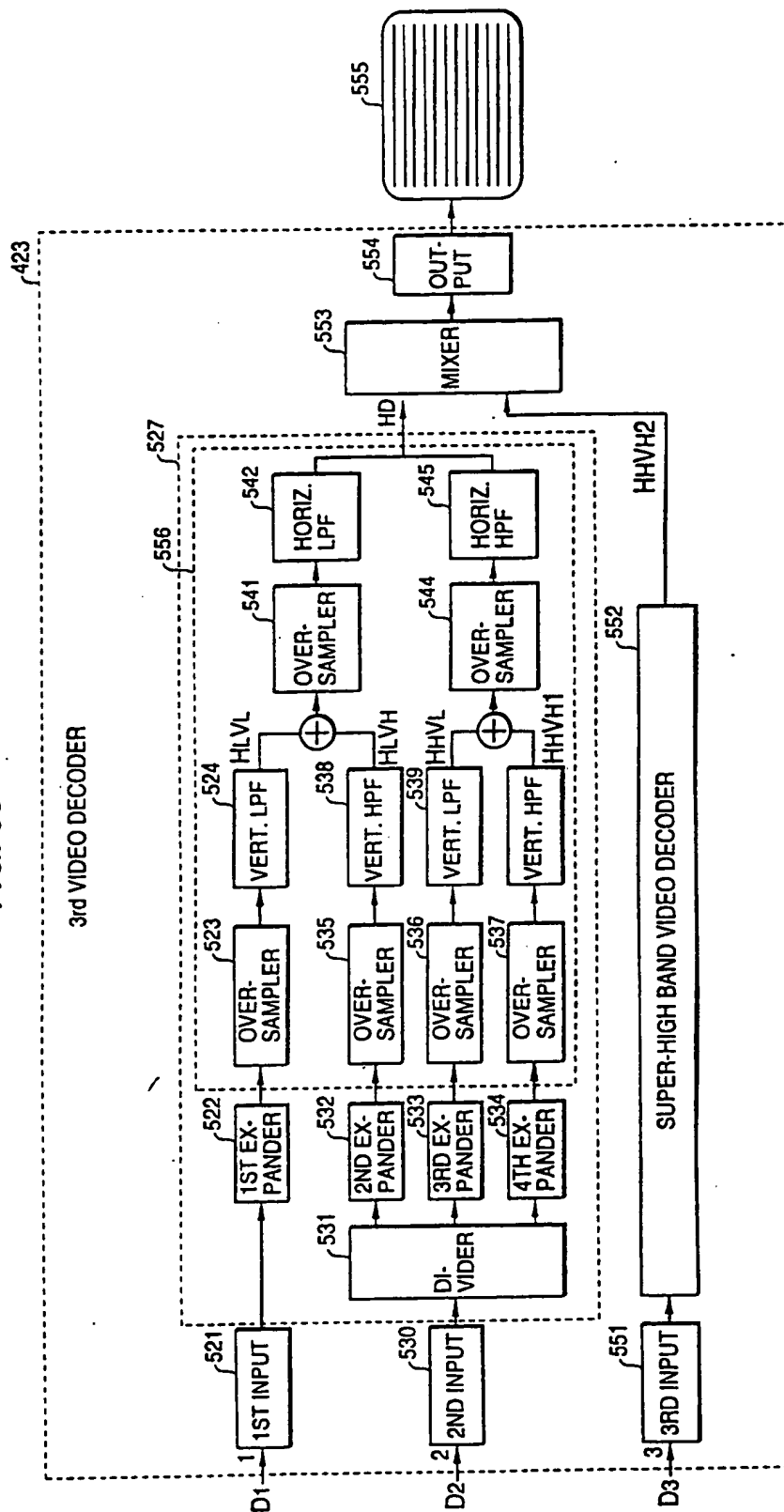


FIG. 34

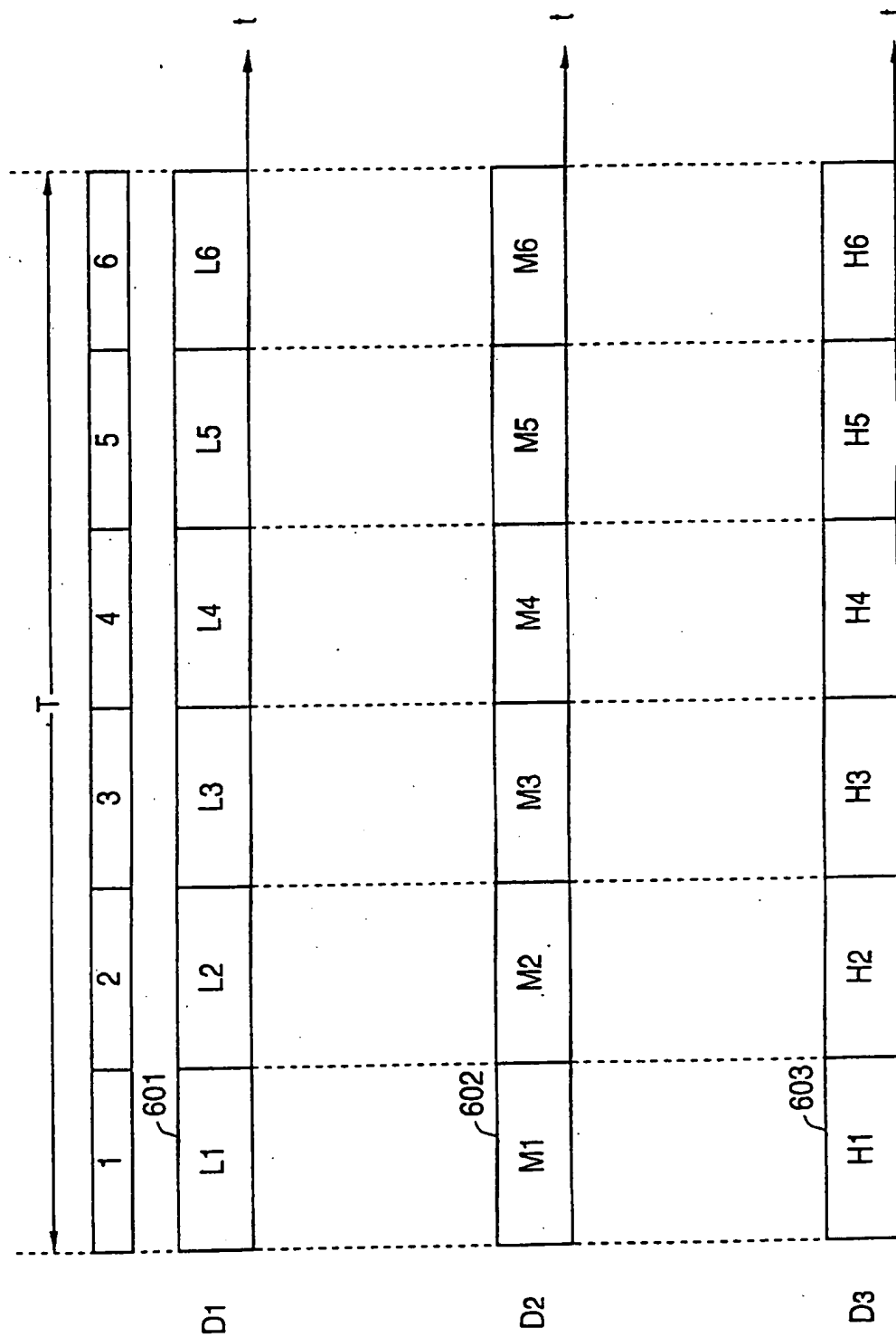


FIG. 35

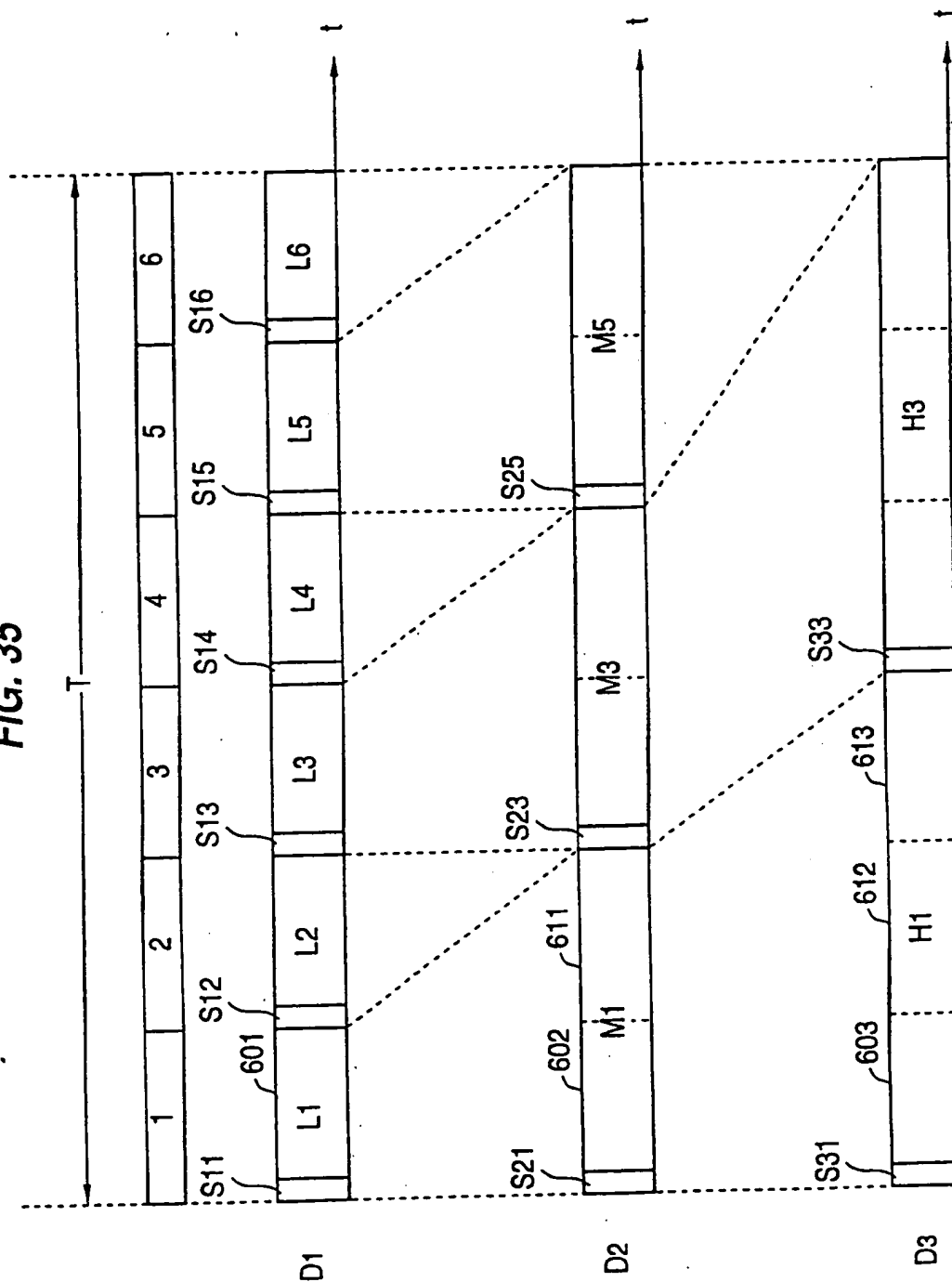


FIG. 36

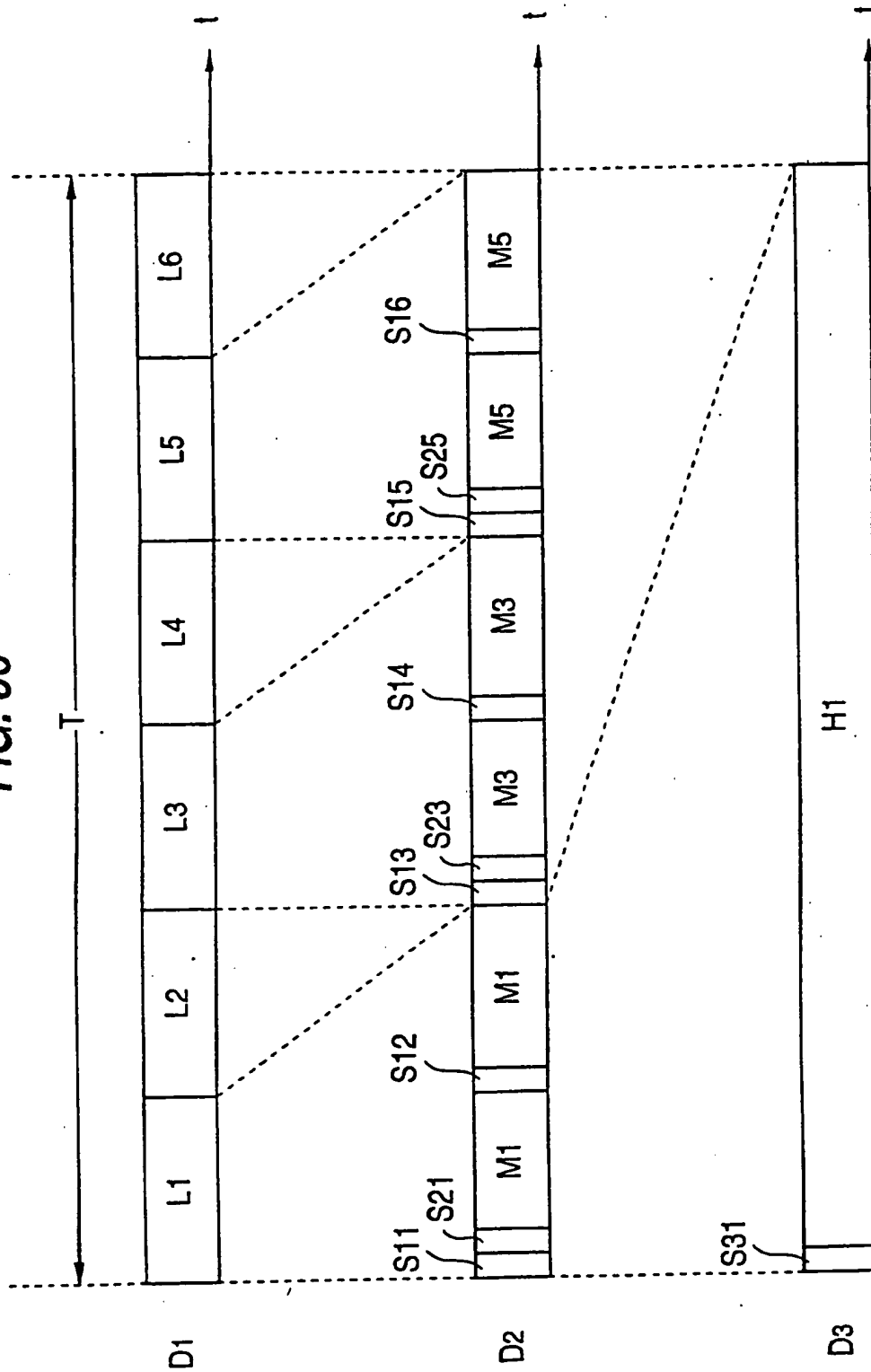


FIG. 37

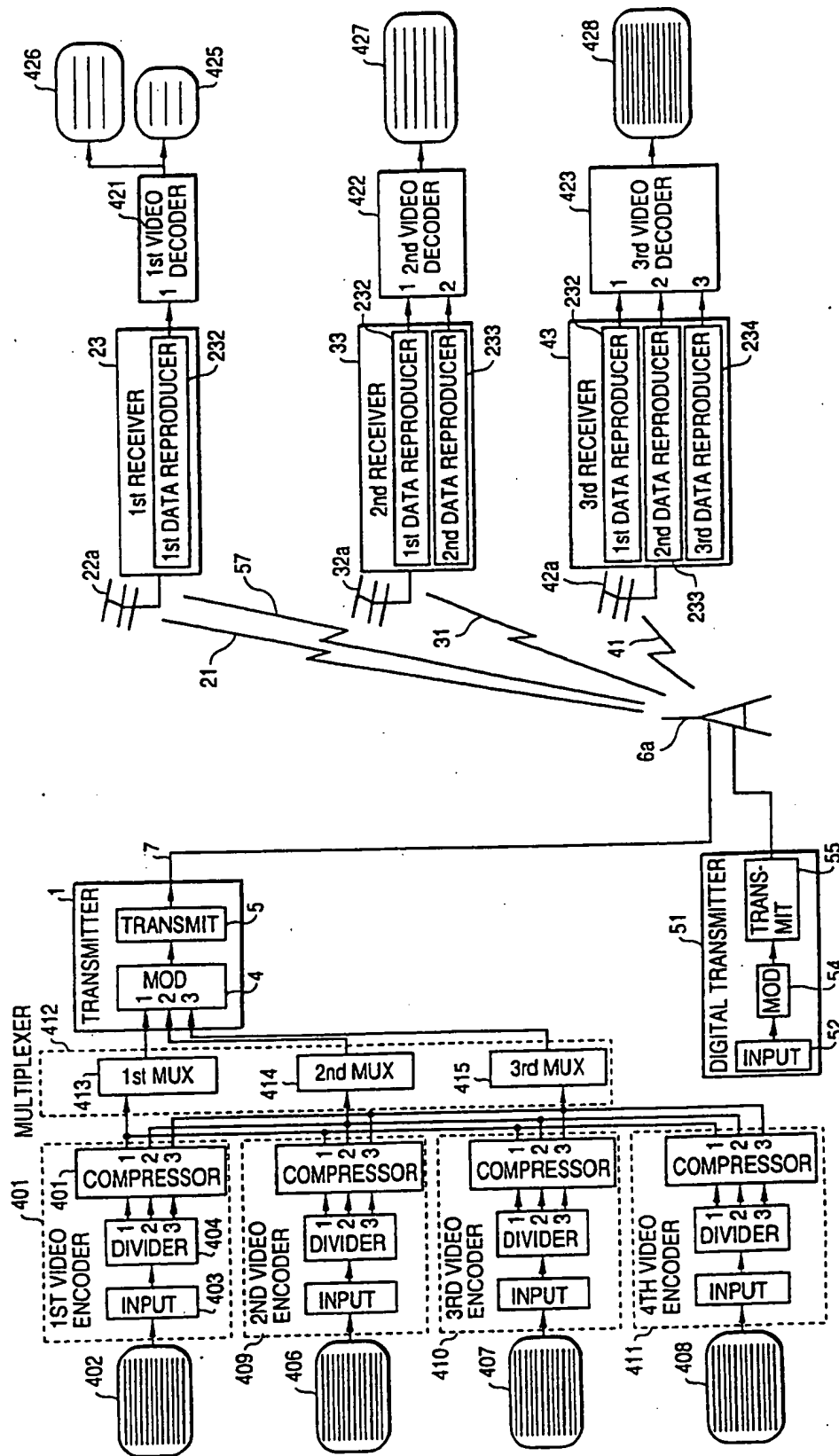


FIG. 38

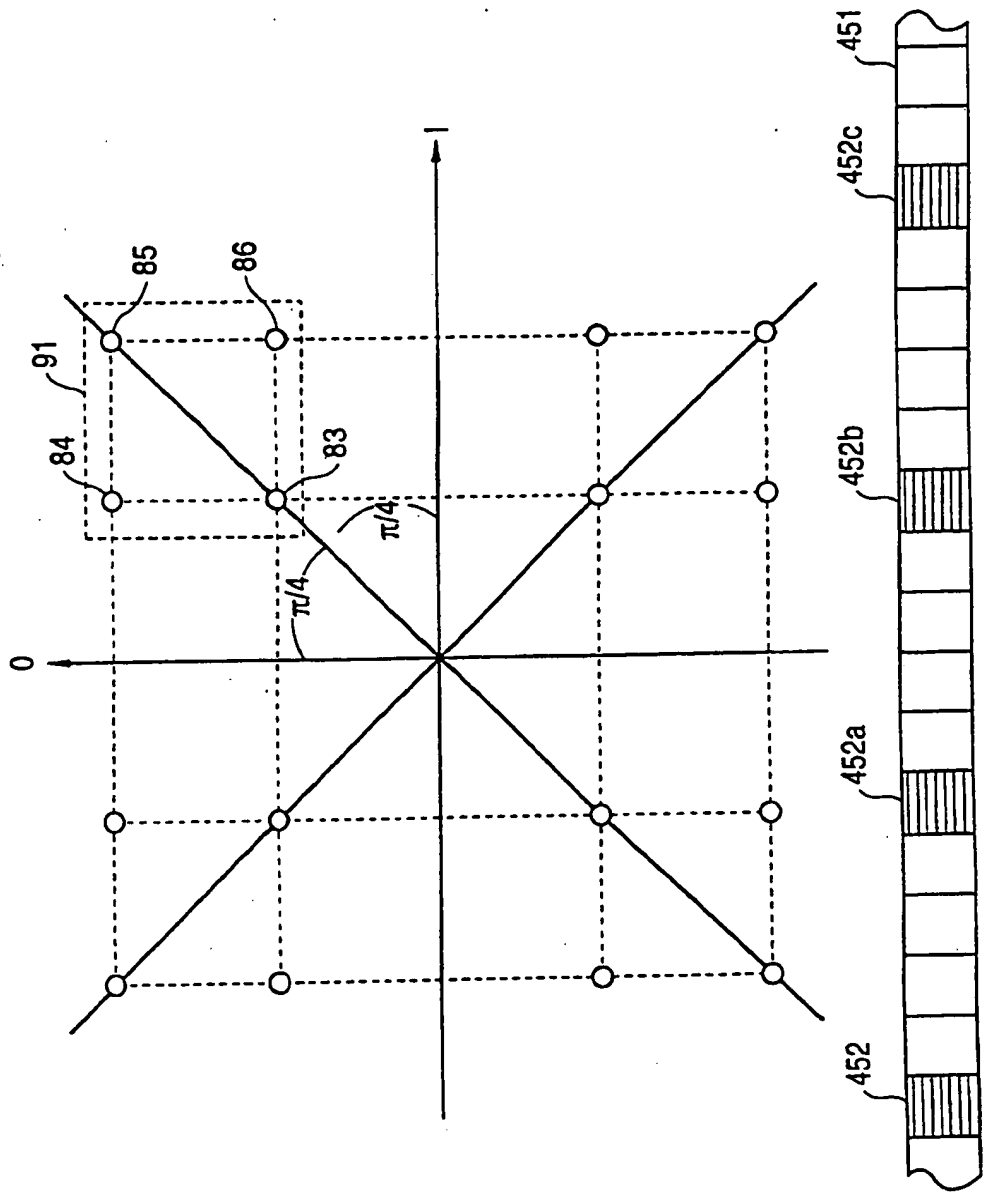
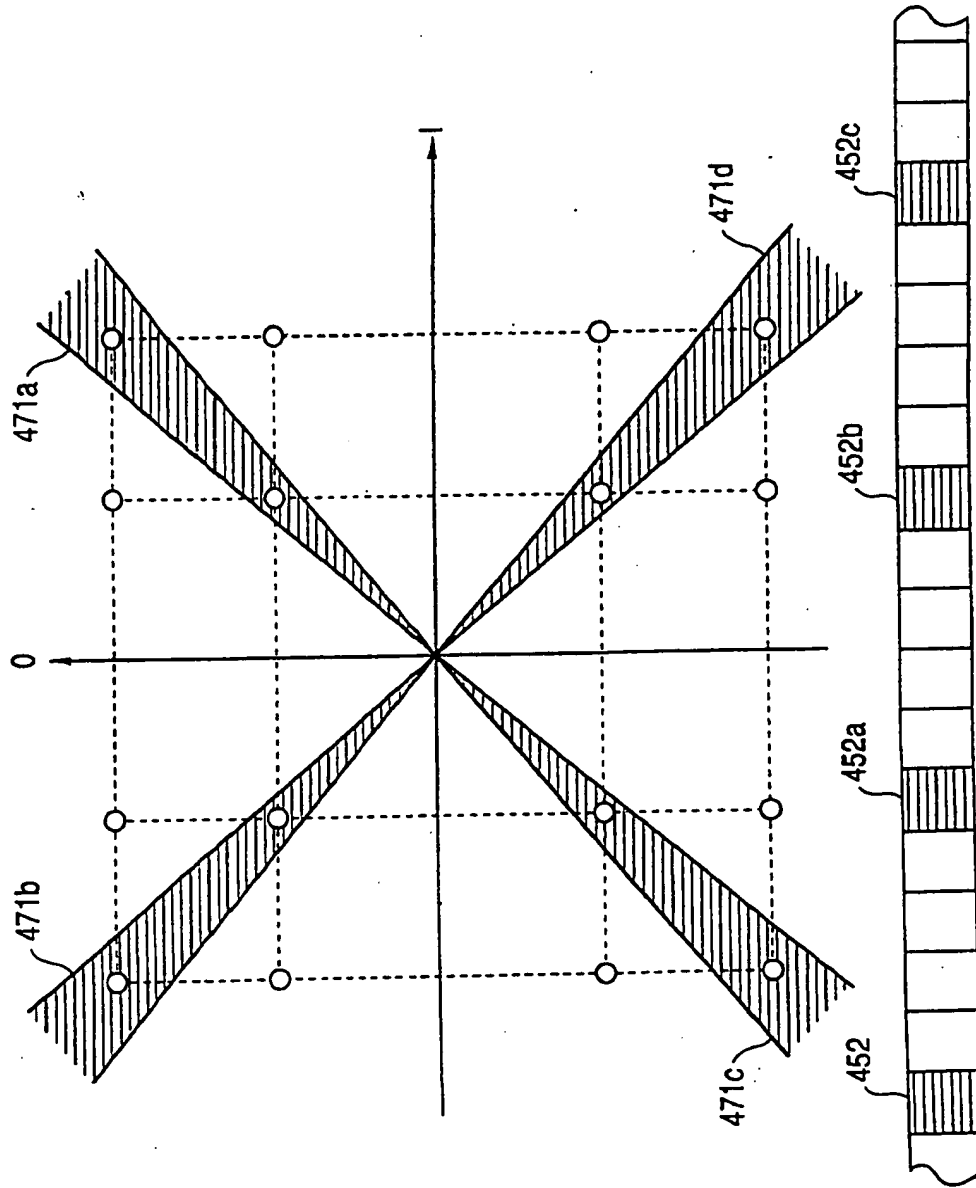
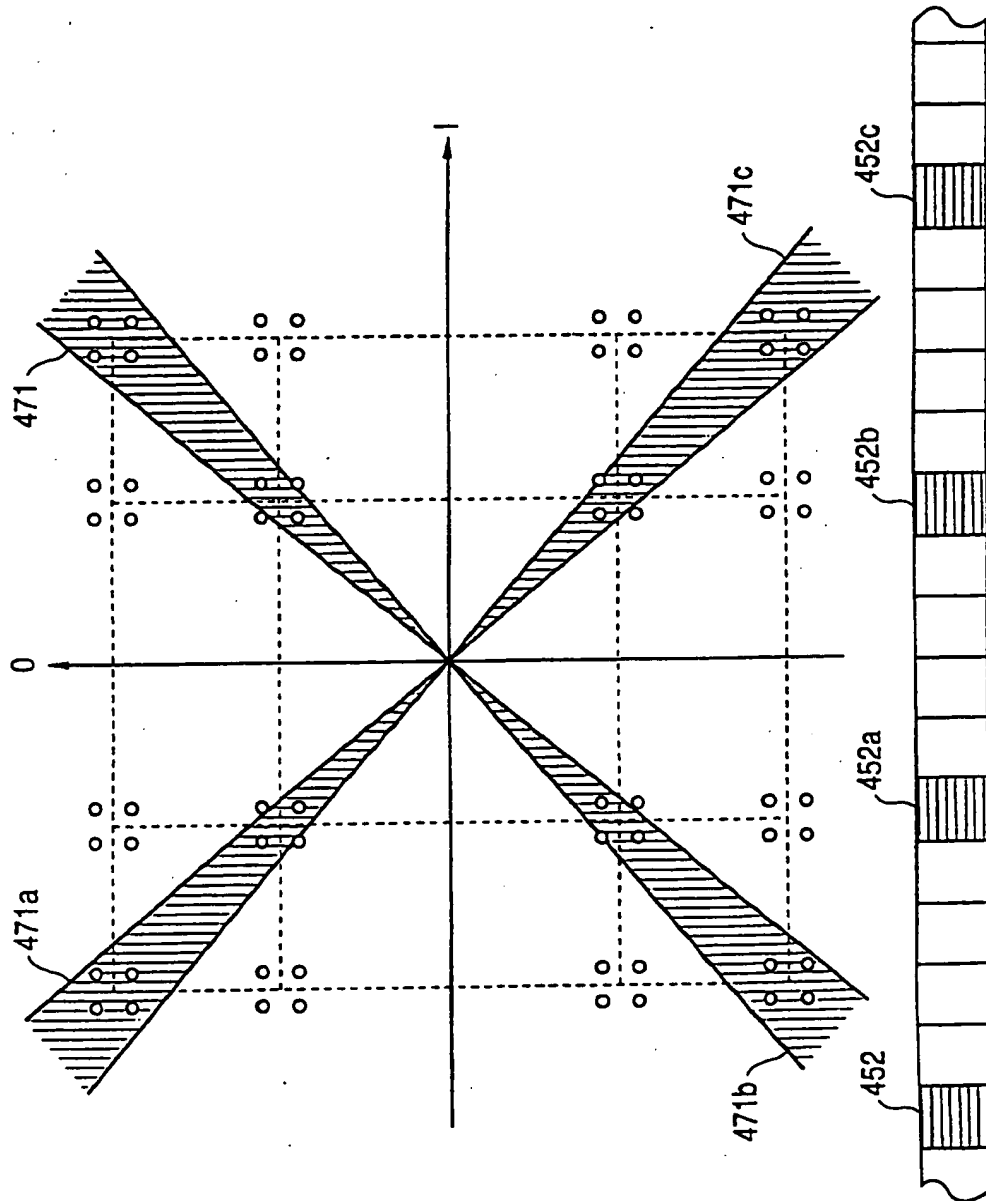


FIG. 39



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FIG. 40



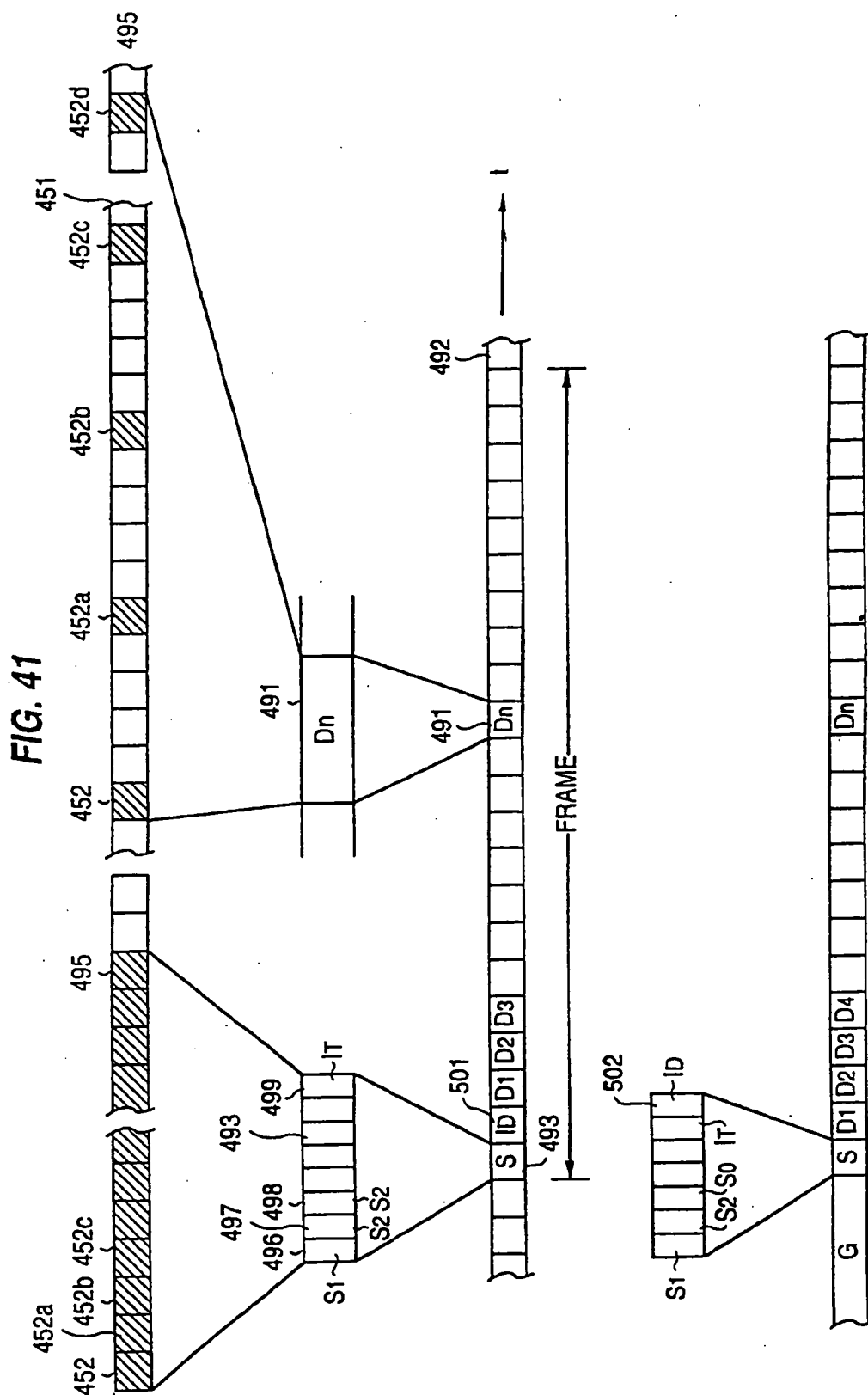


FIG. 42

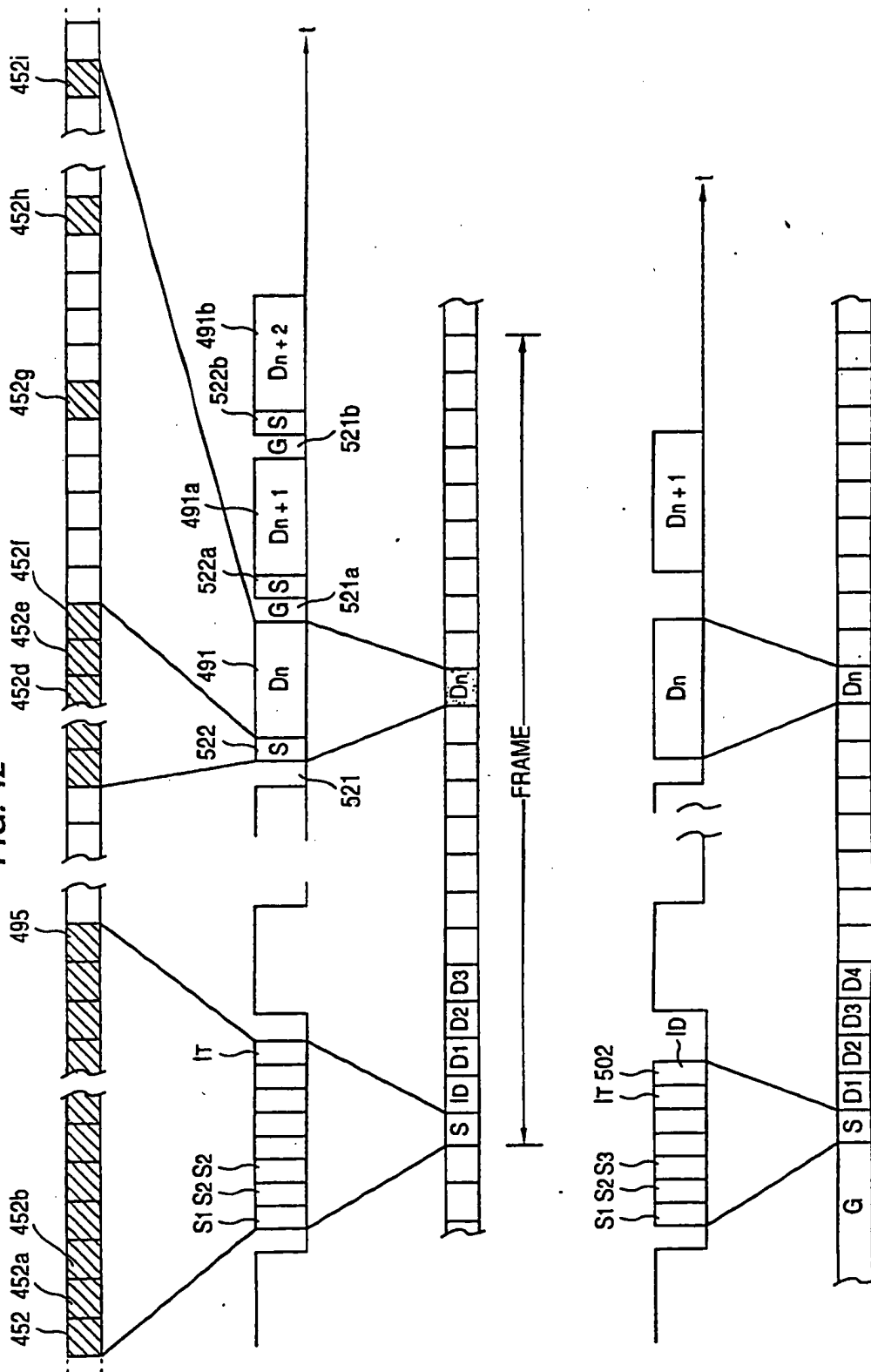
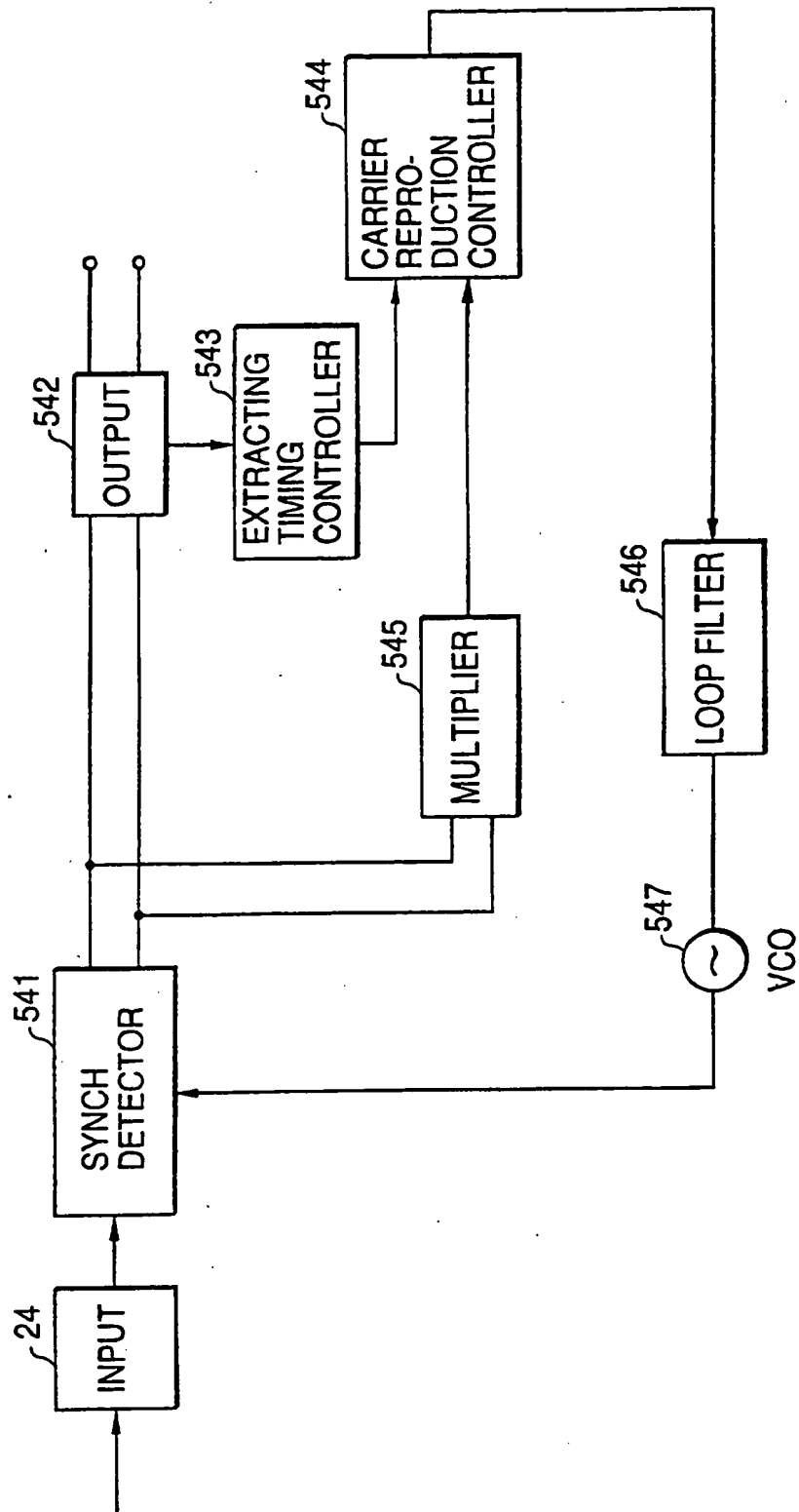


FIG. 43



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FIG. 44

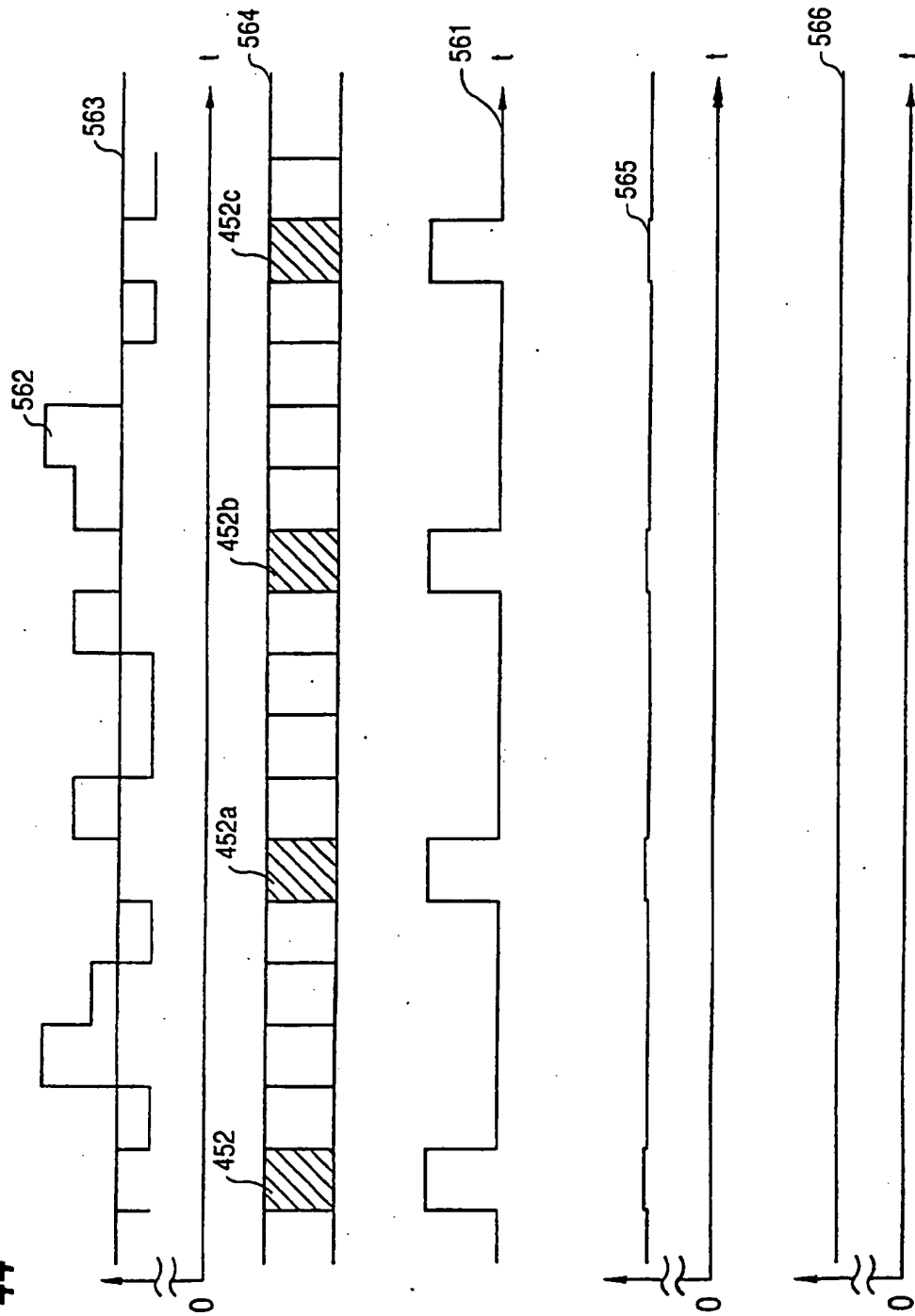


FIG. 45

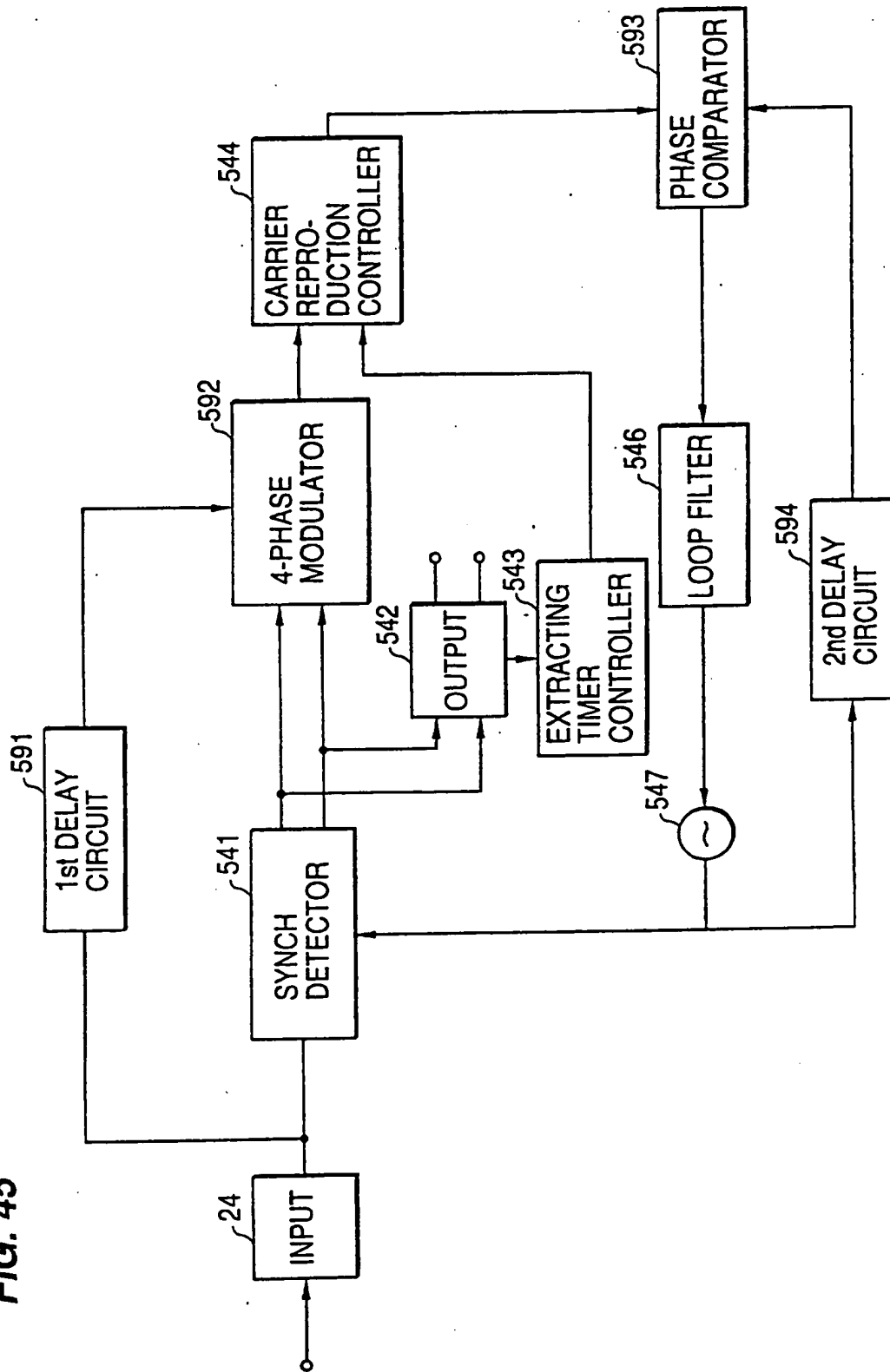


FIG. 46

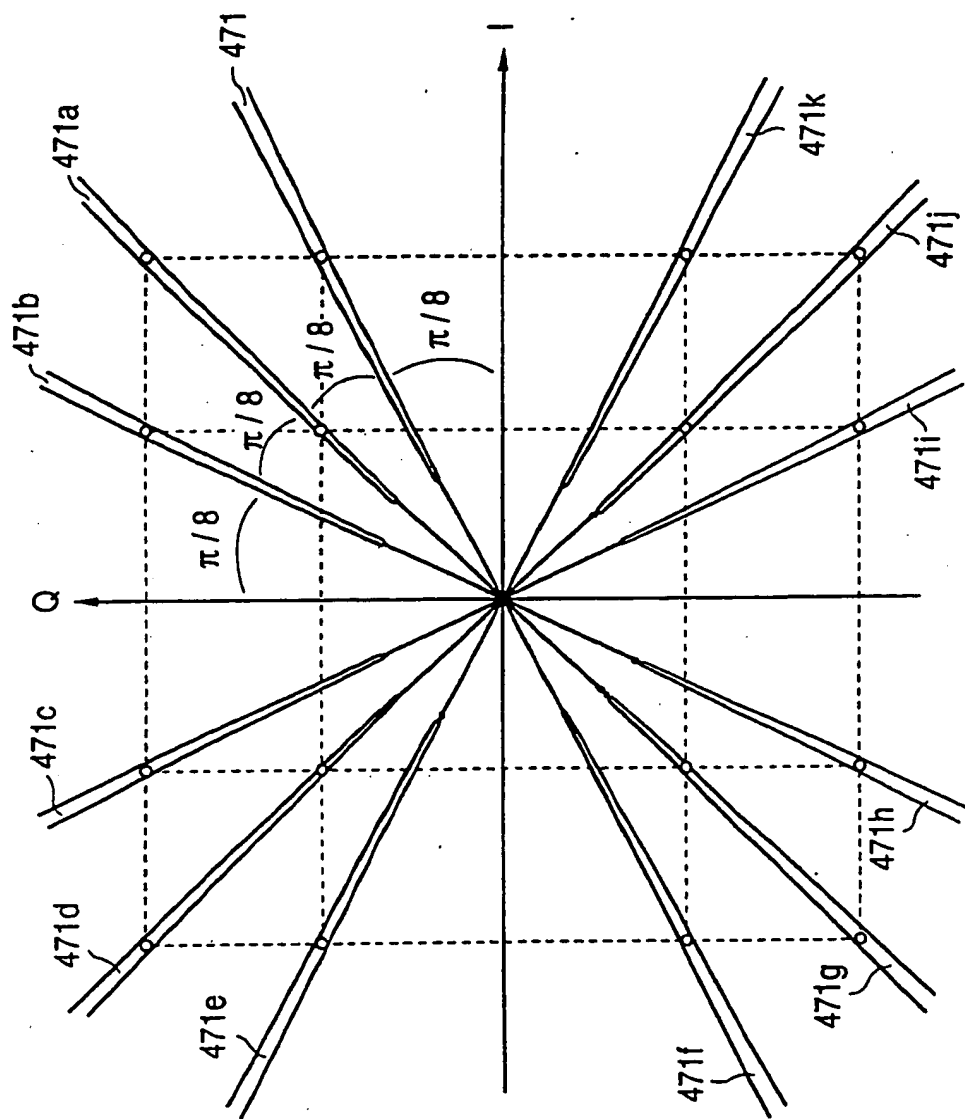


FIG. 47

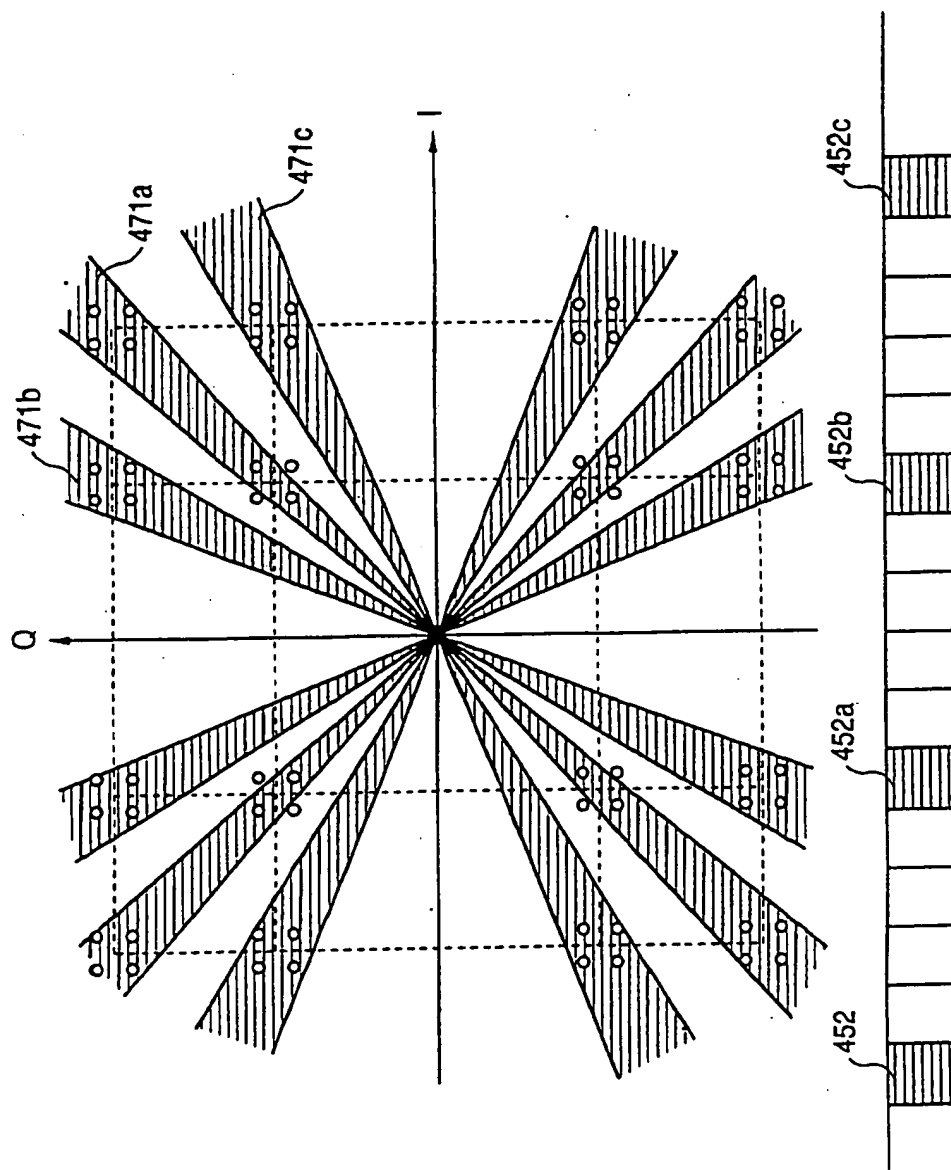


FIG. 48

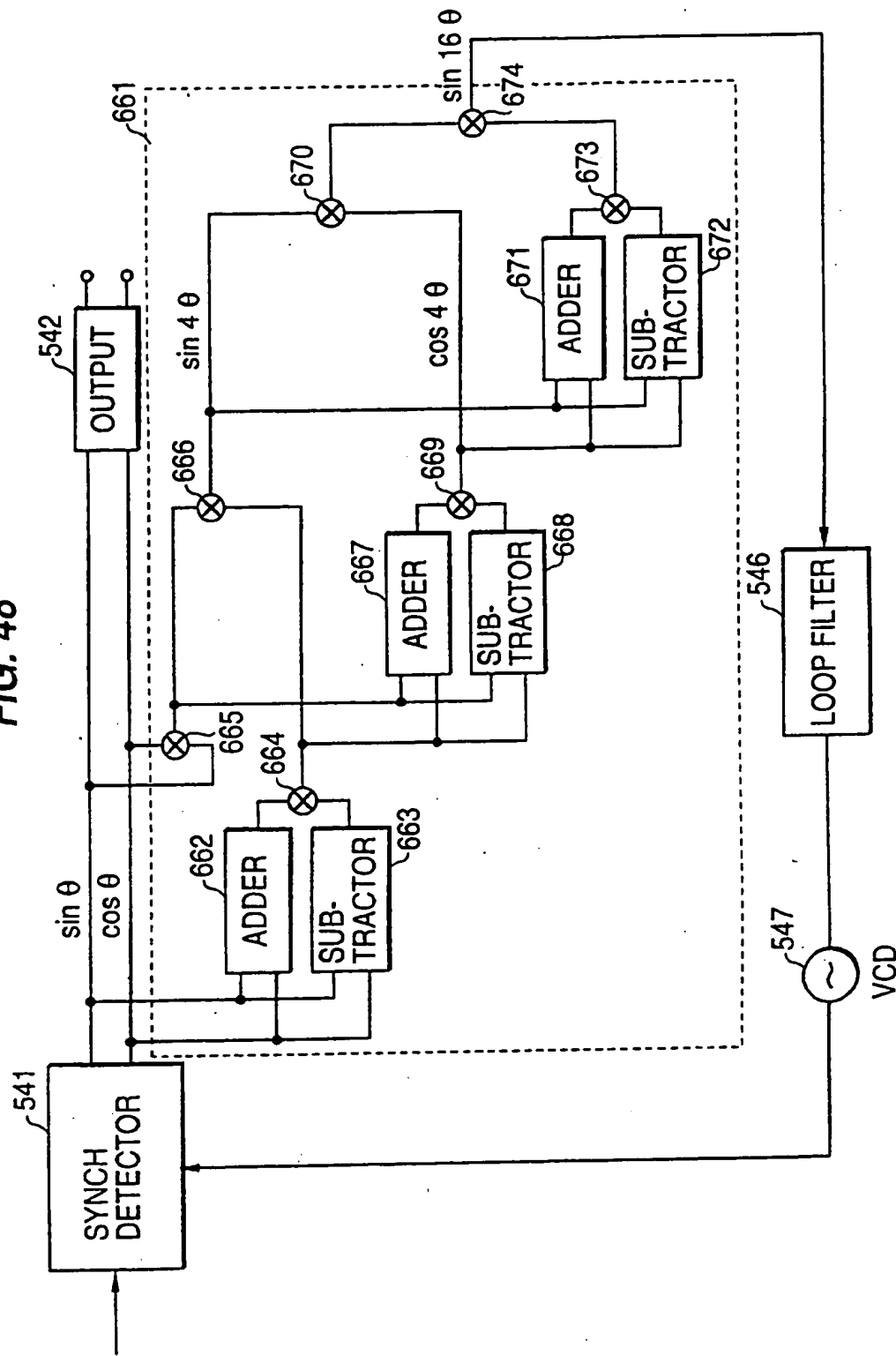


FIG. 49

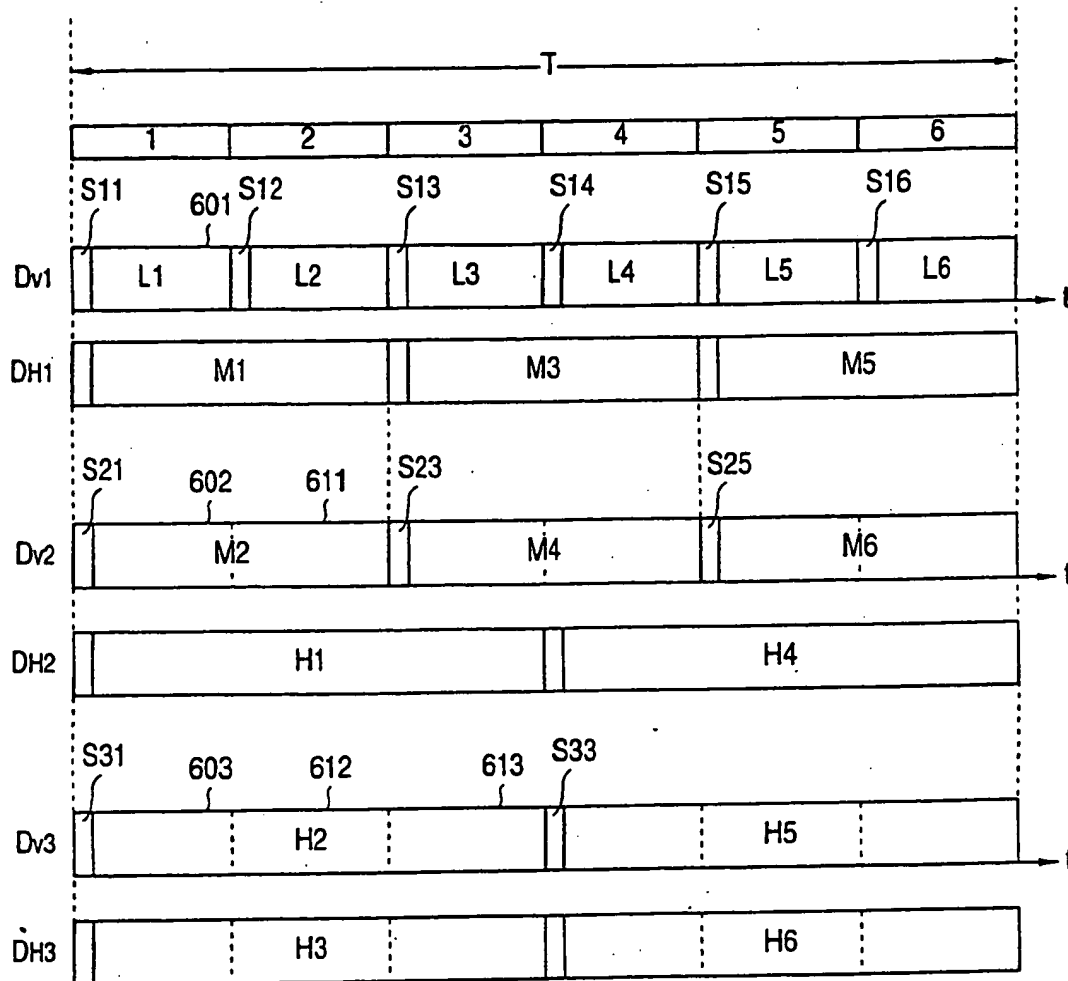
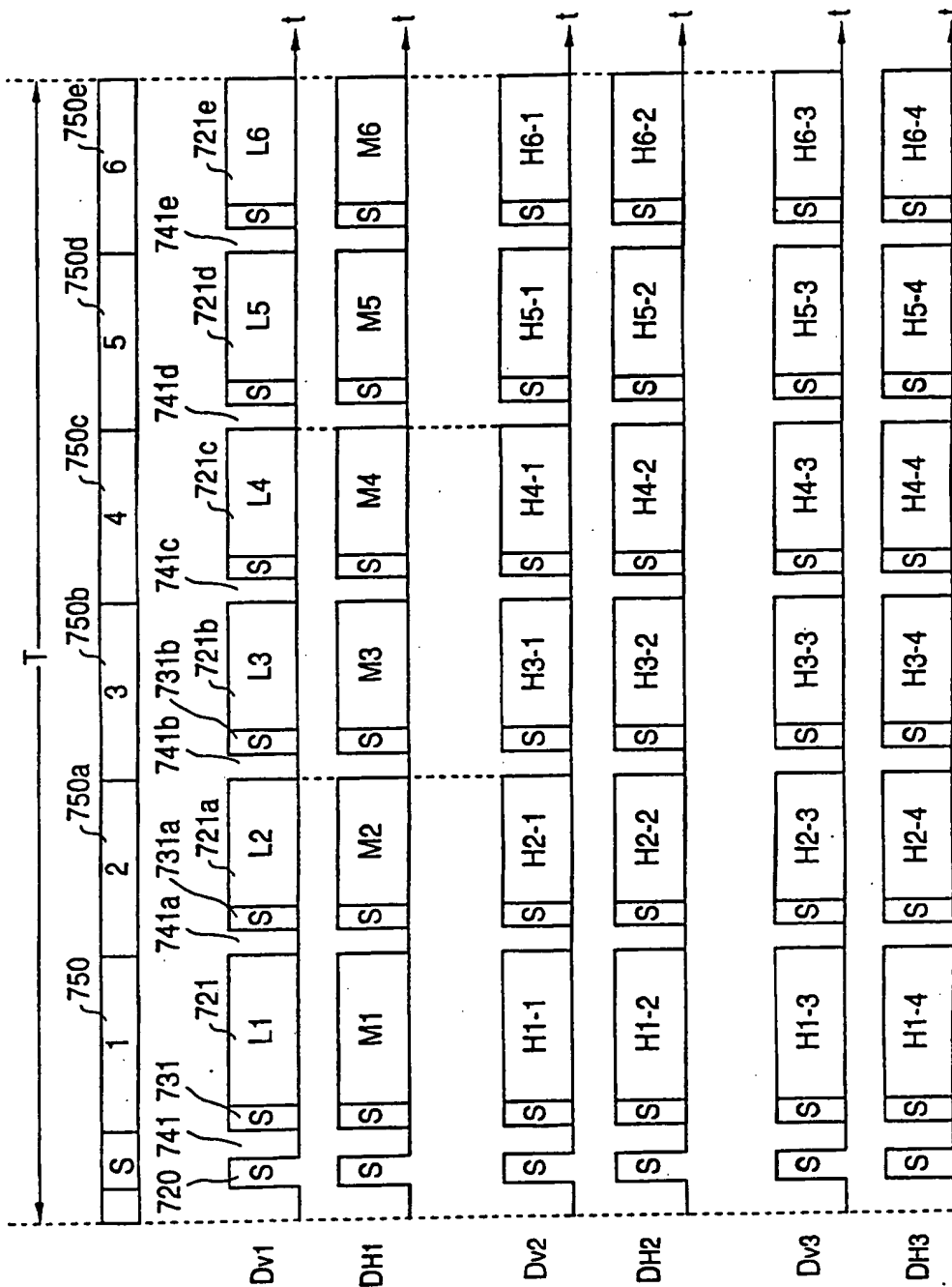


FIG. 50



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FIG. 51

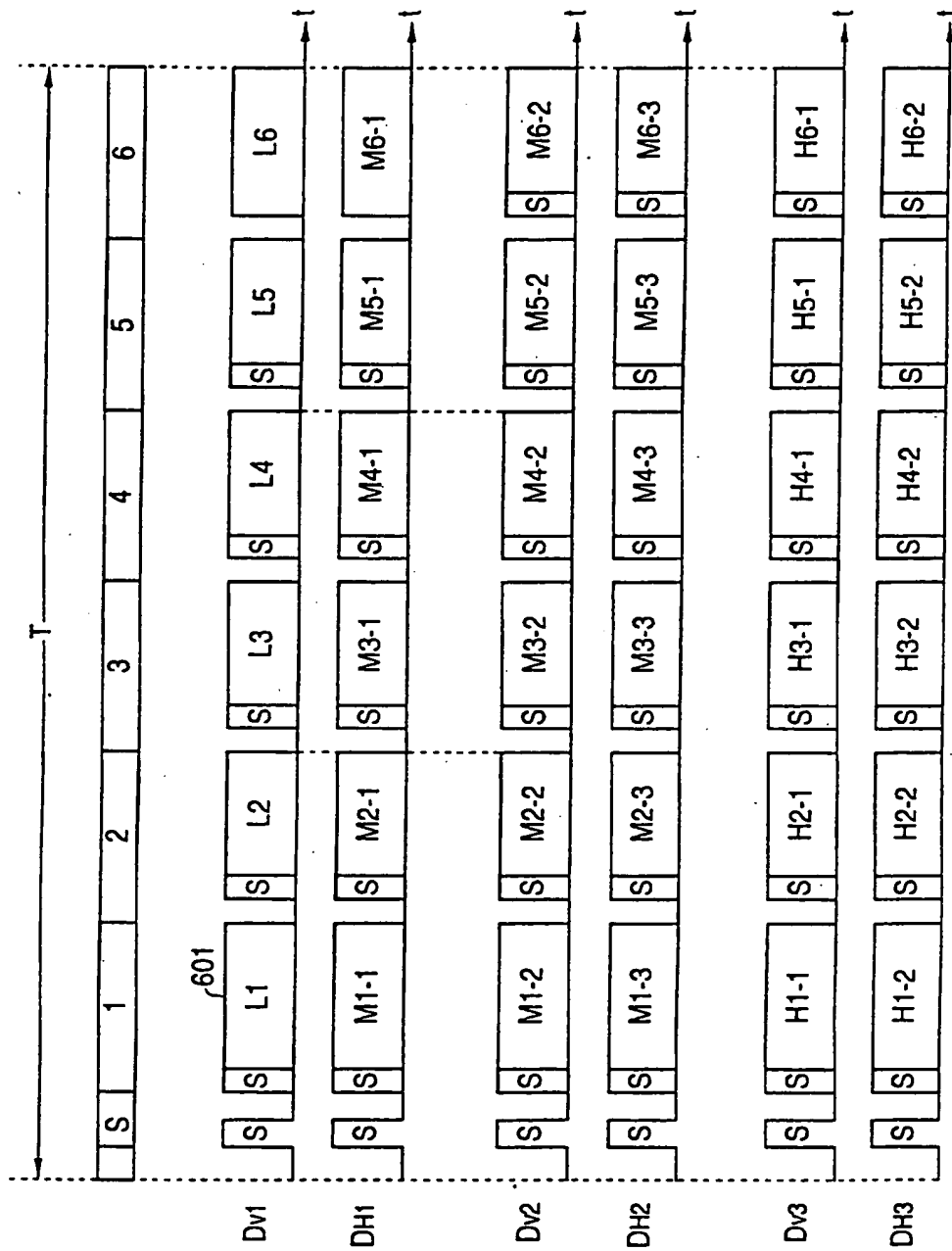
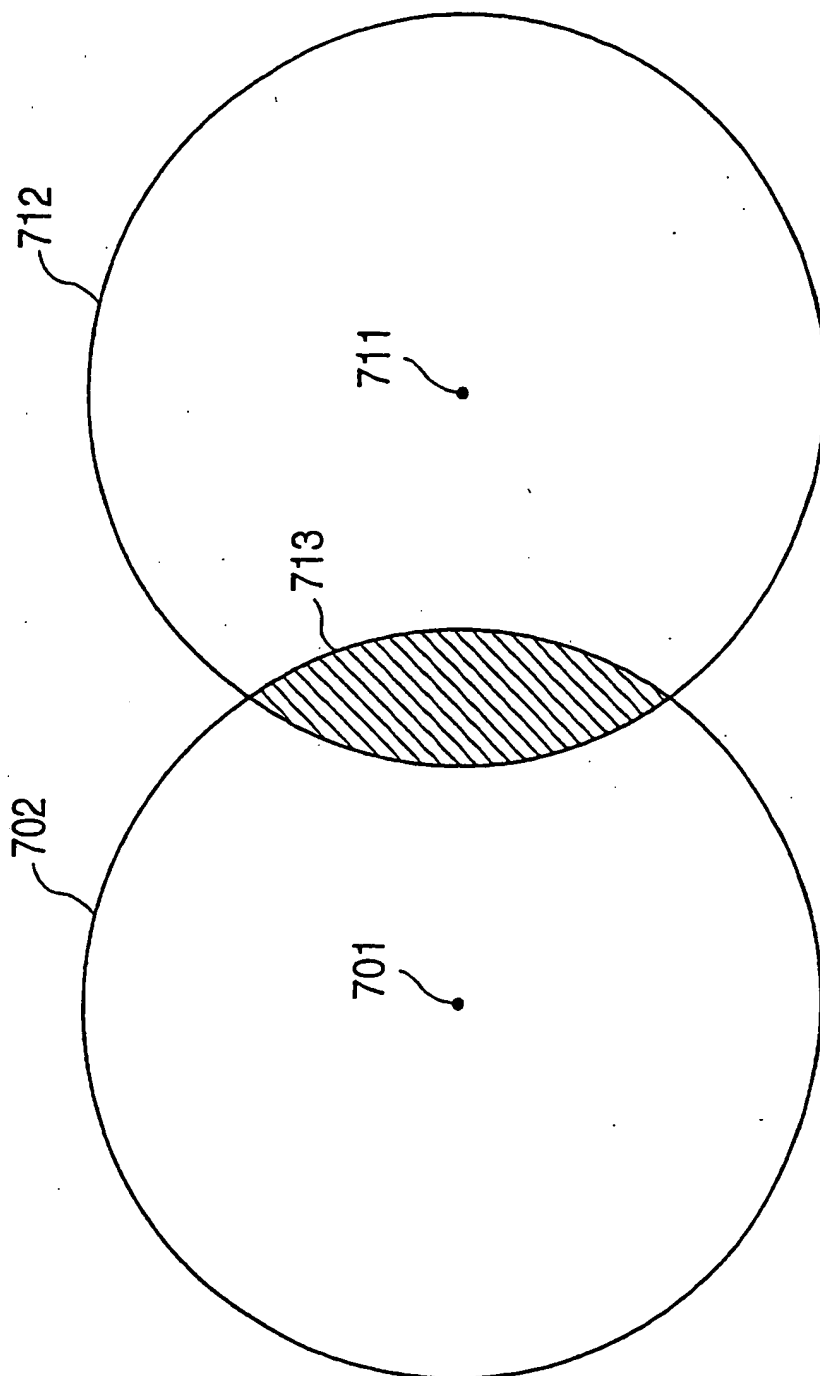
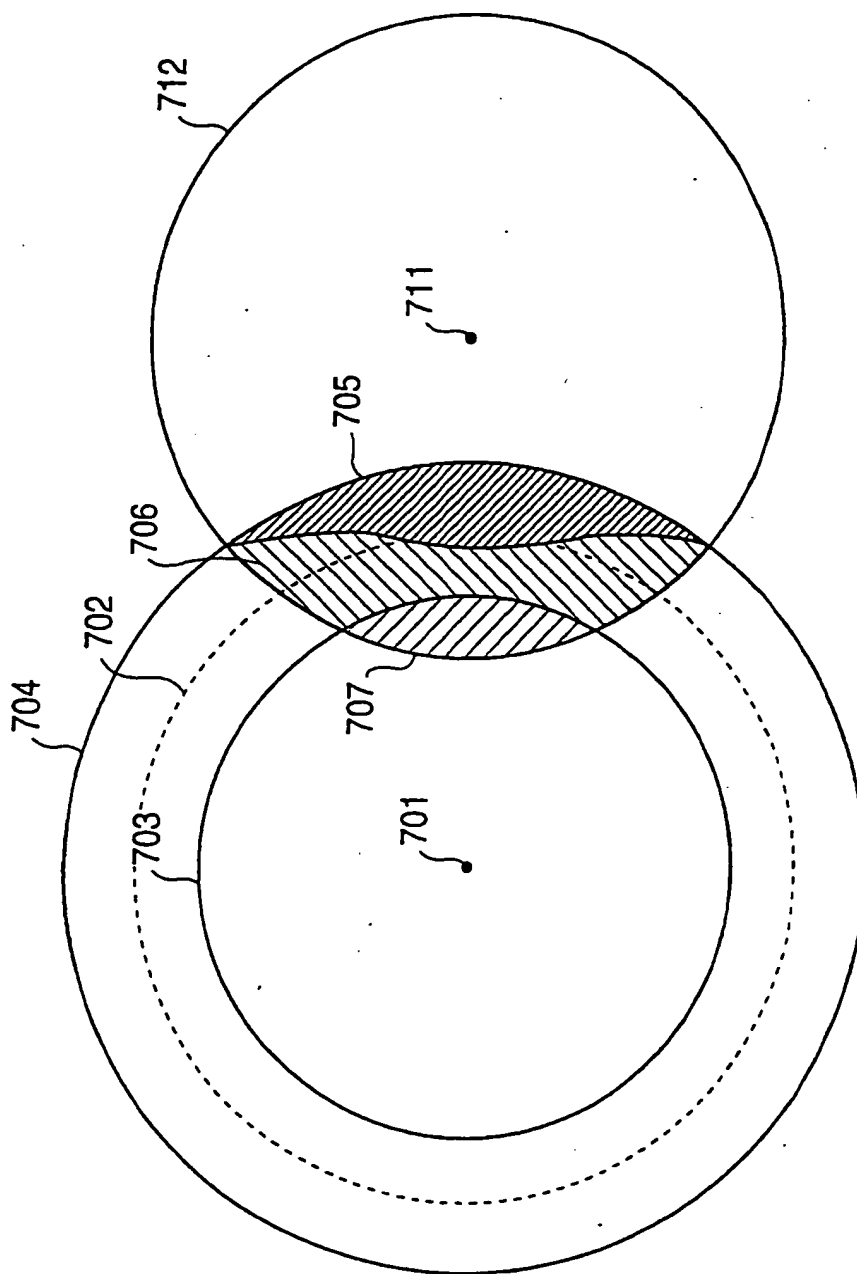


FIG. 52



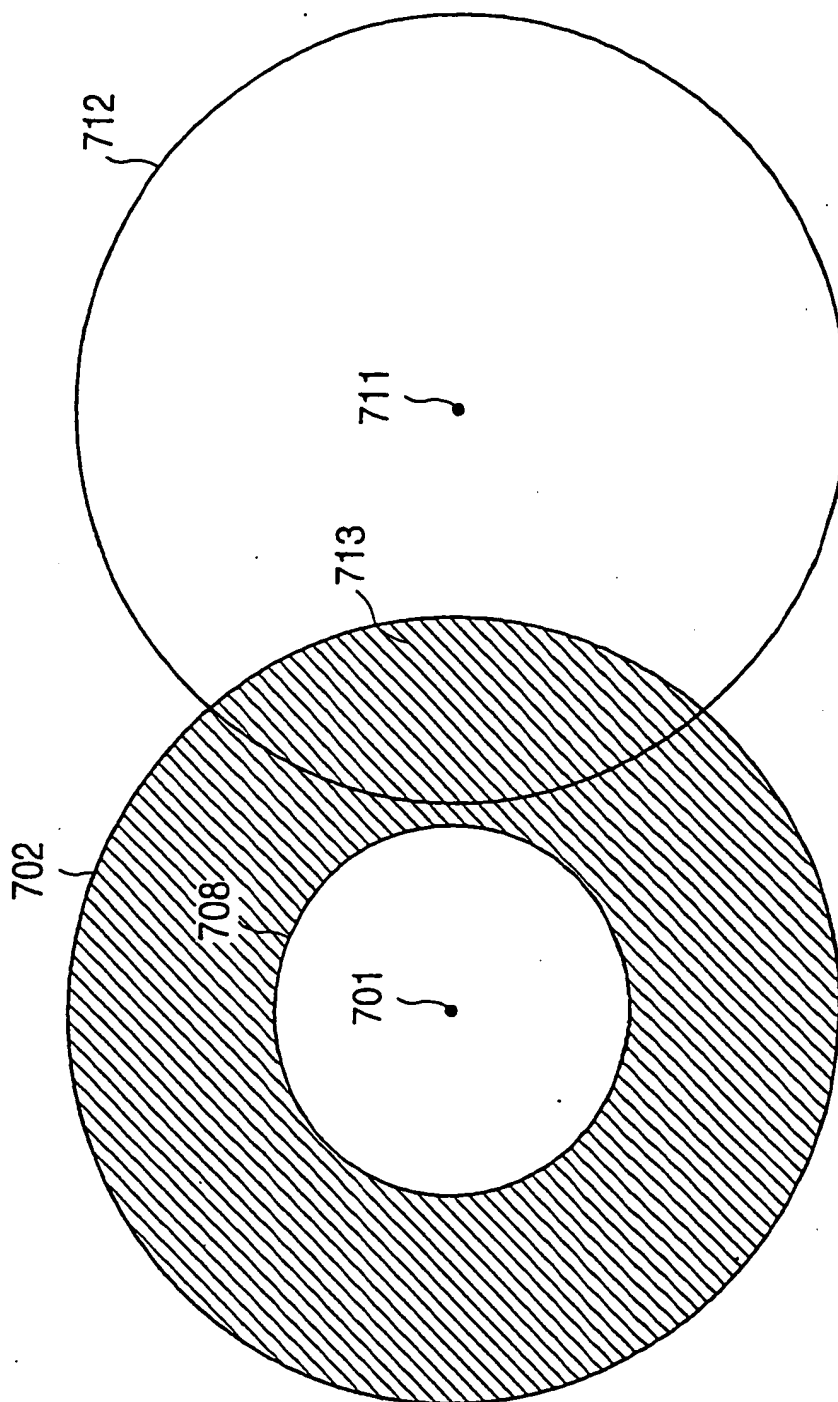
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FIG. 53



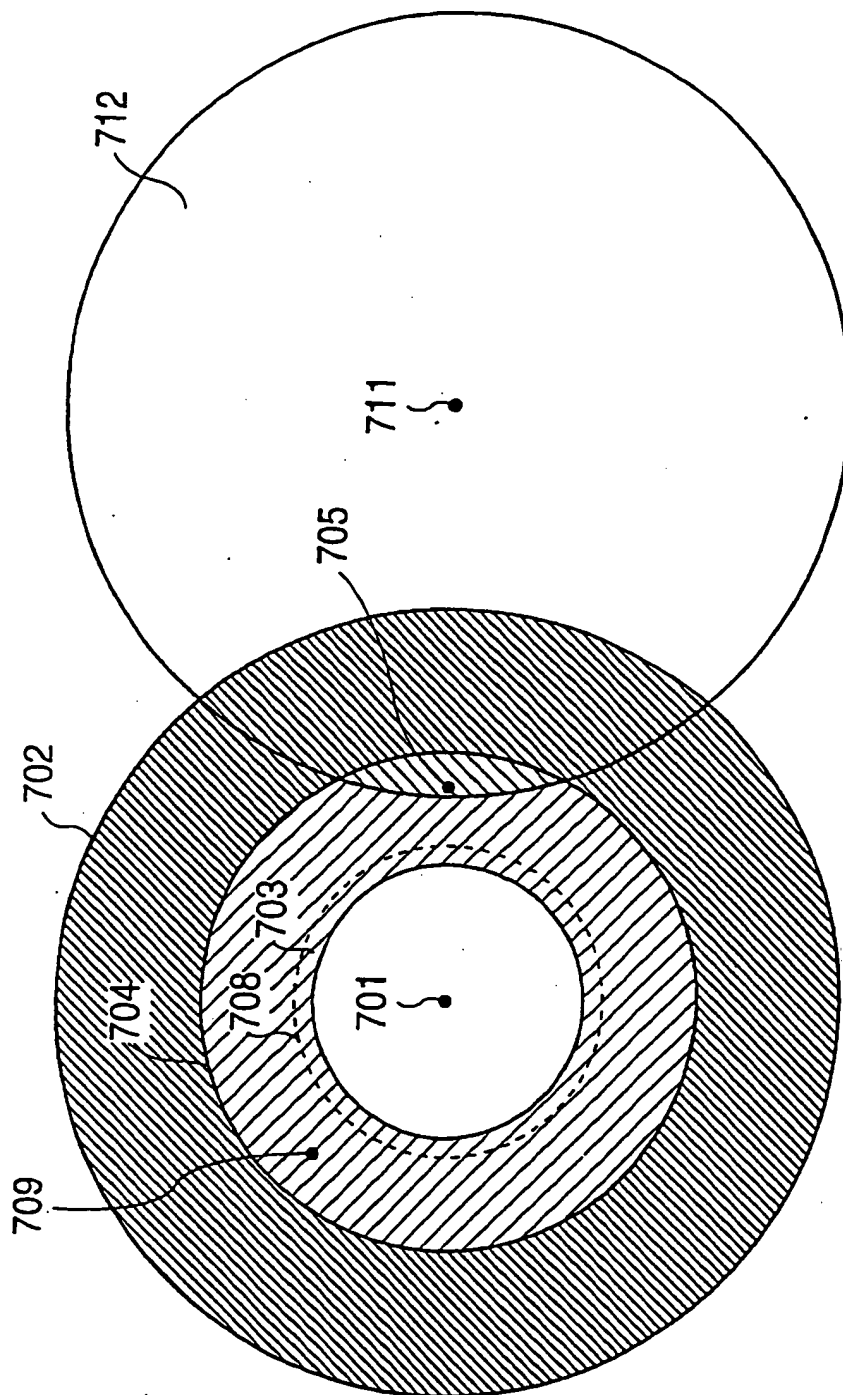
005037 2/1996

FIG. 54



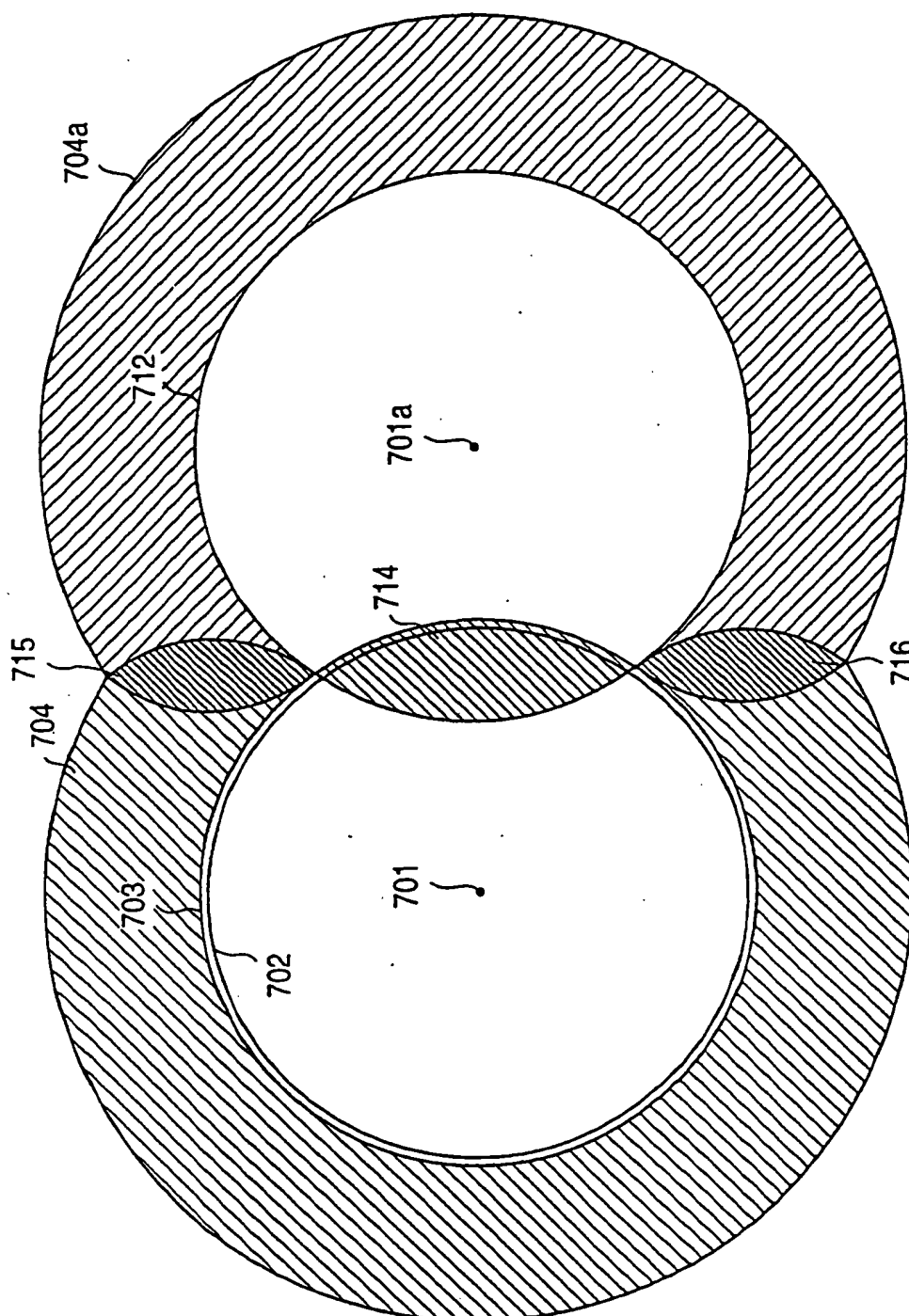
005001 / 100000

FIG. 55



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FIG. 56



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FIG. 57

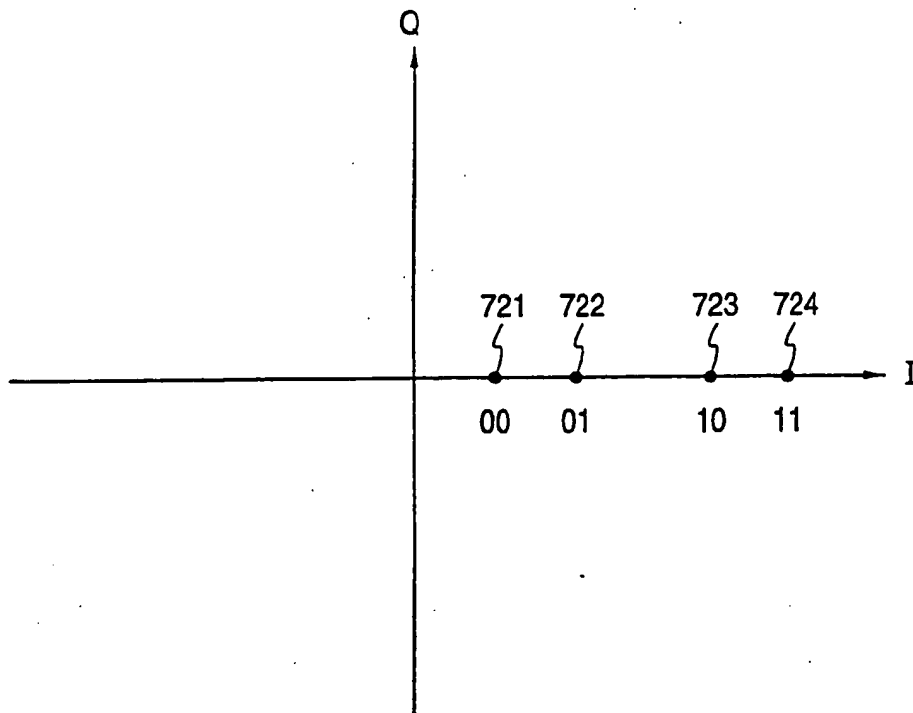


FIG. 58

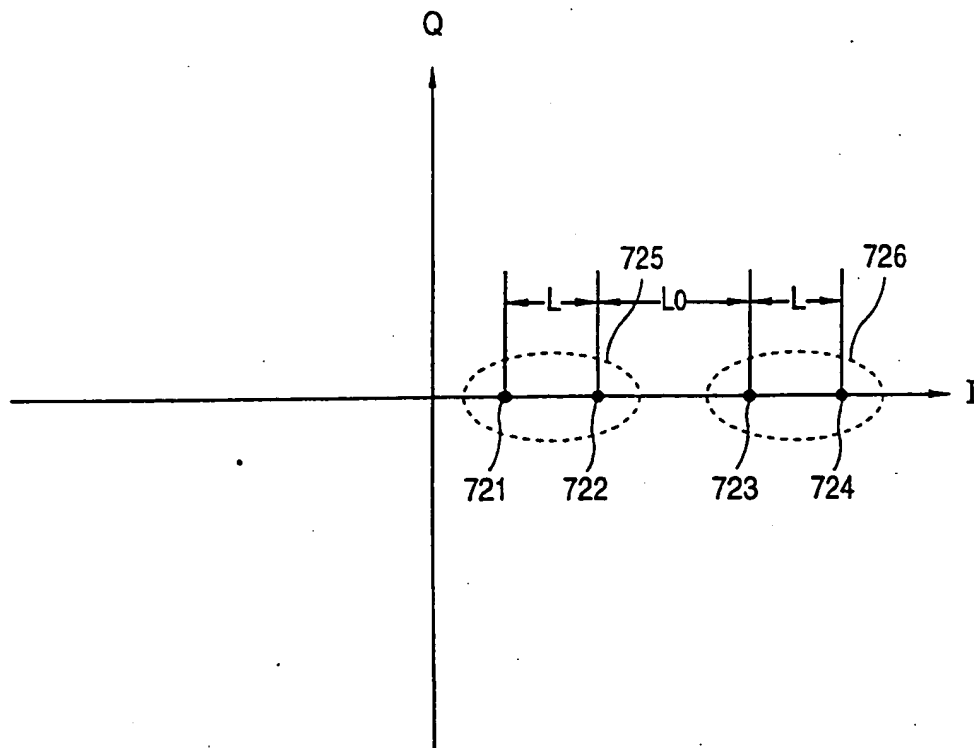


FIG. 59(a)

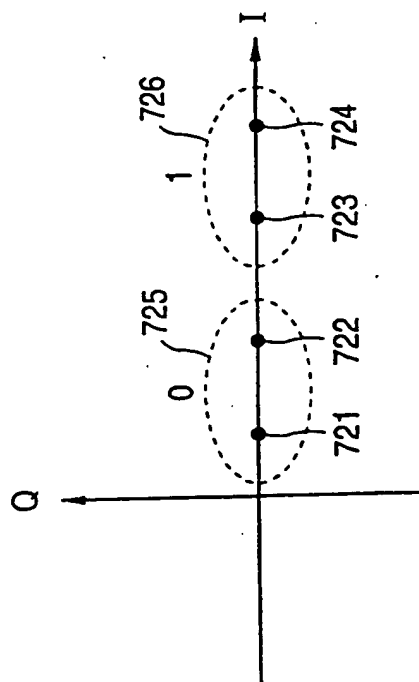


FIG. 59(b)

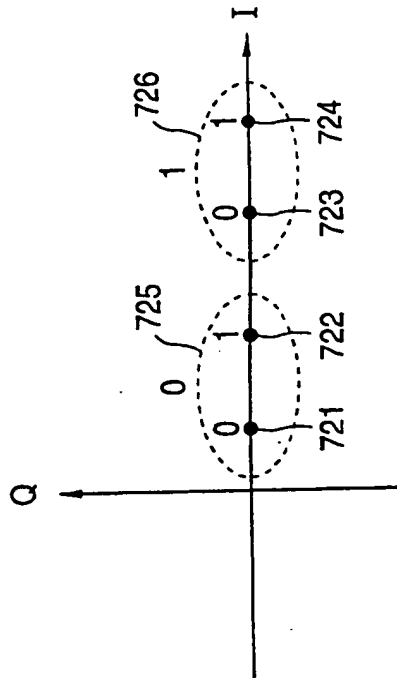


FIG. 59(c)

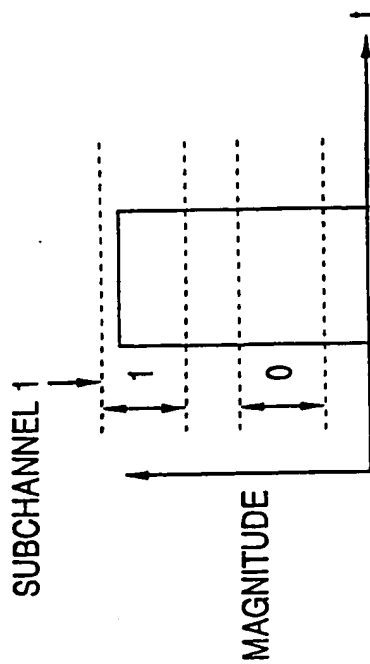
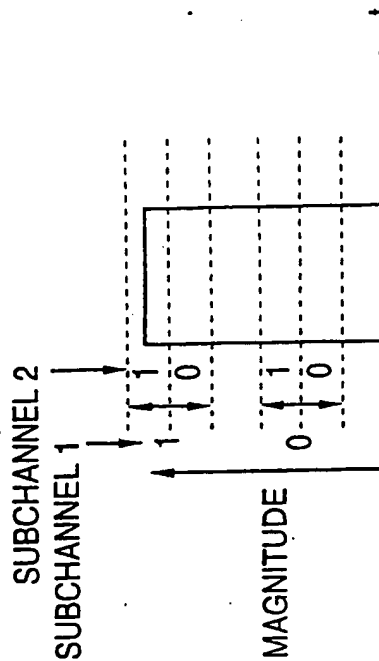
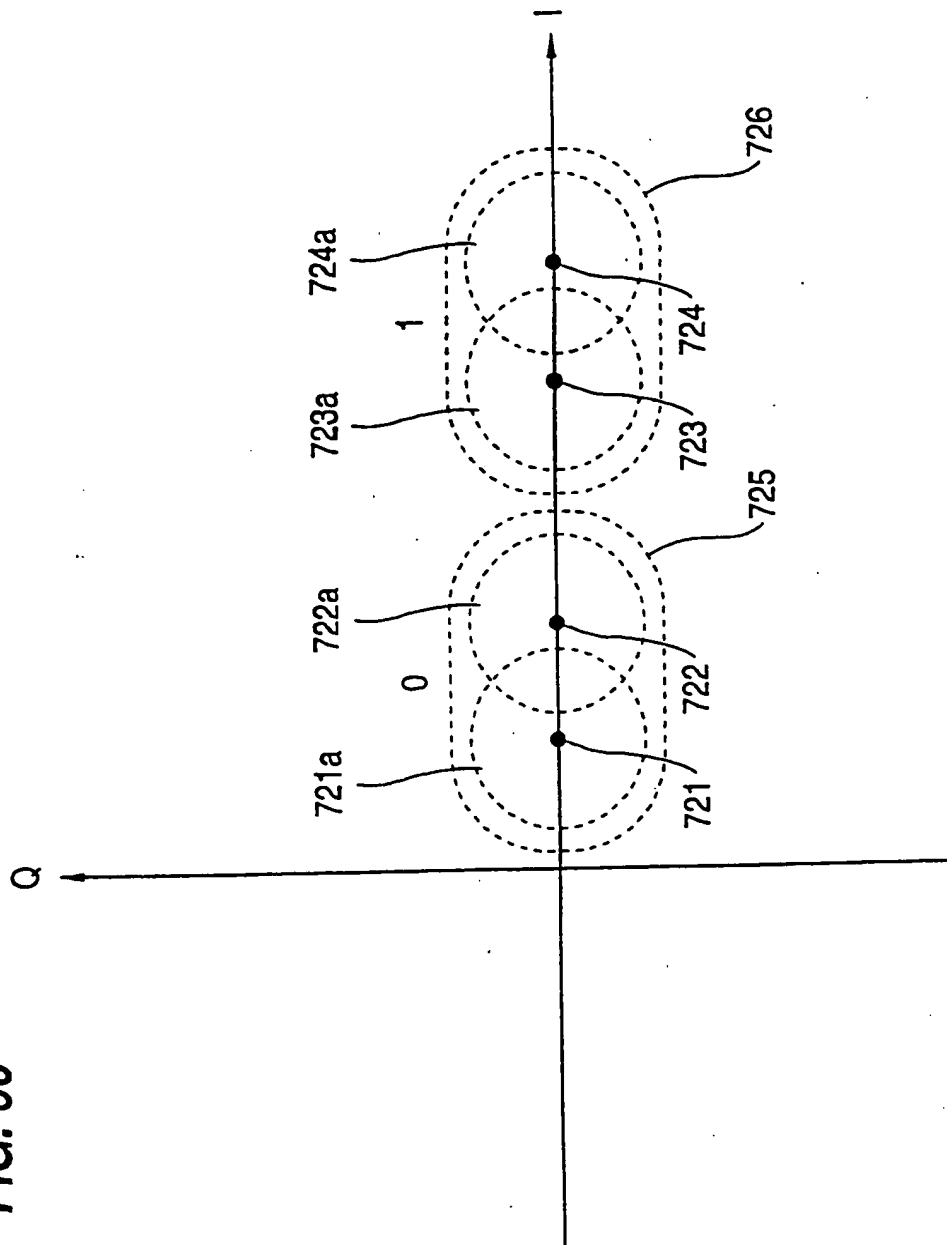


FIG. 59(d)



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FIG. 60



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FIG. 61

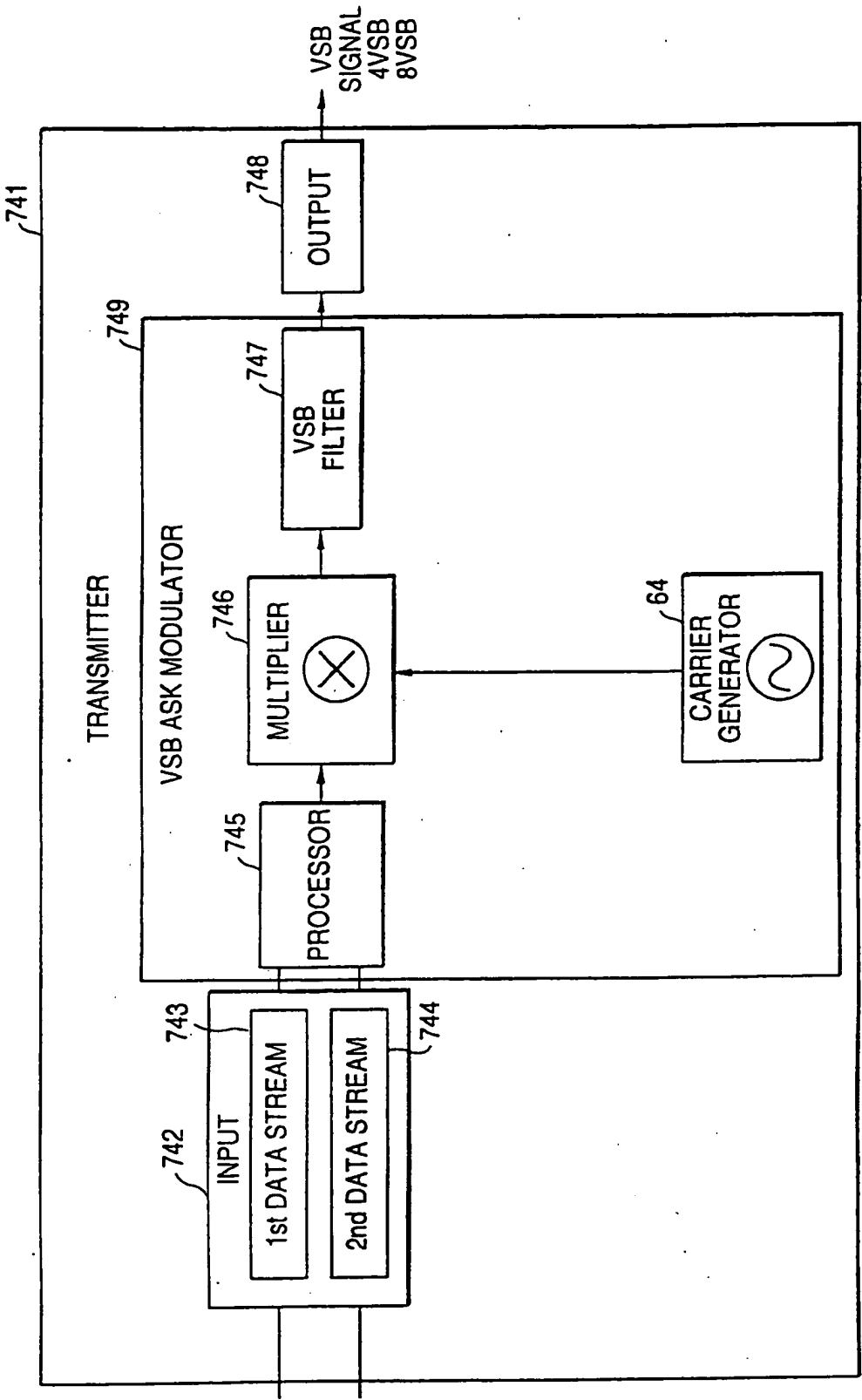


FIG. 62(a)

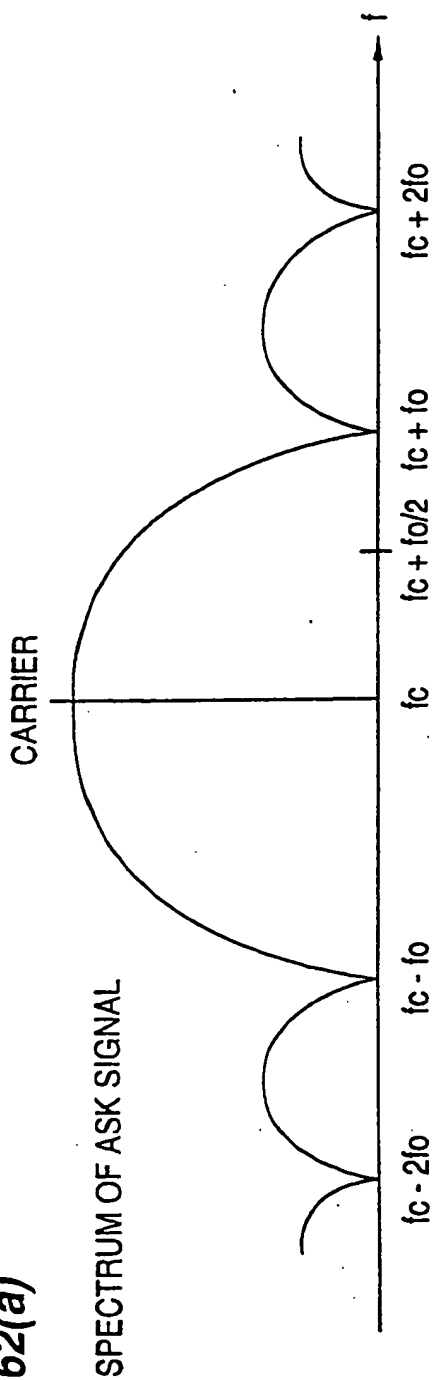


FIG. 62(b)

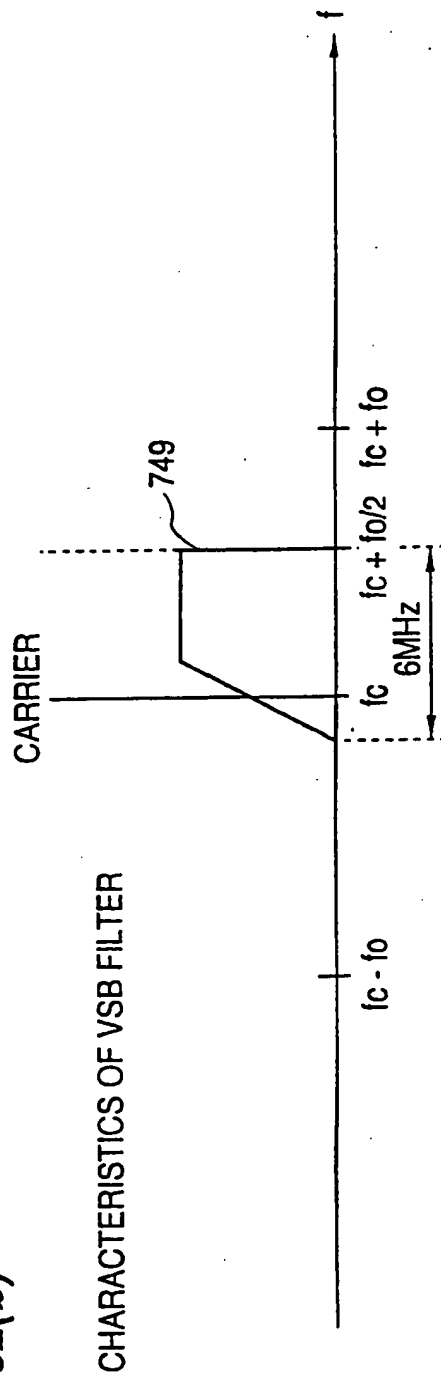


FIG. 63

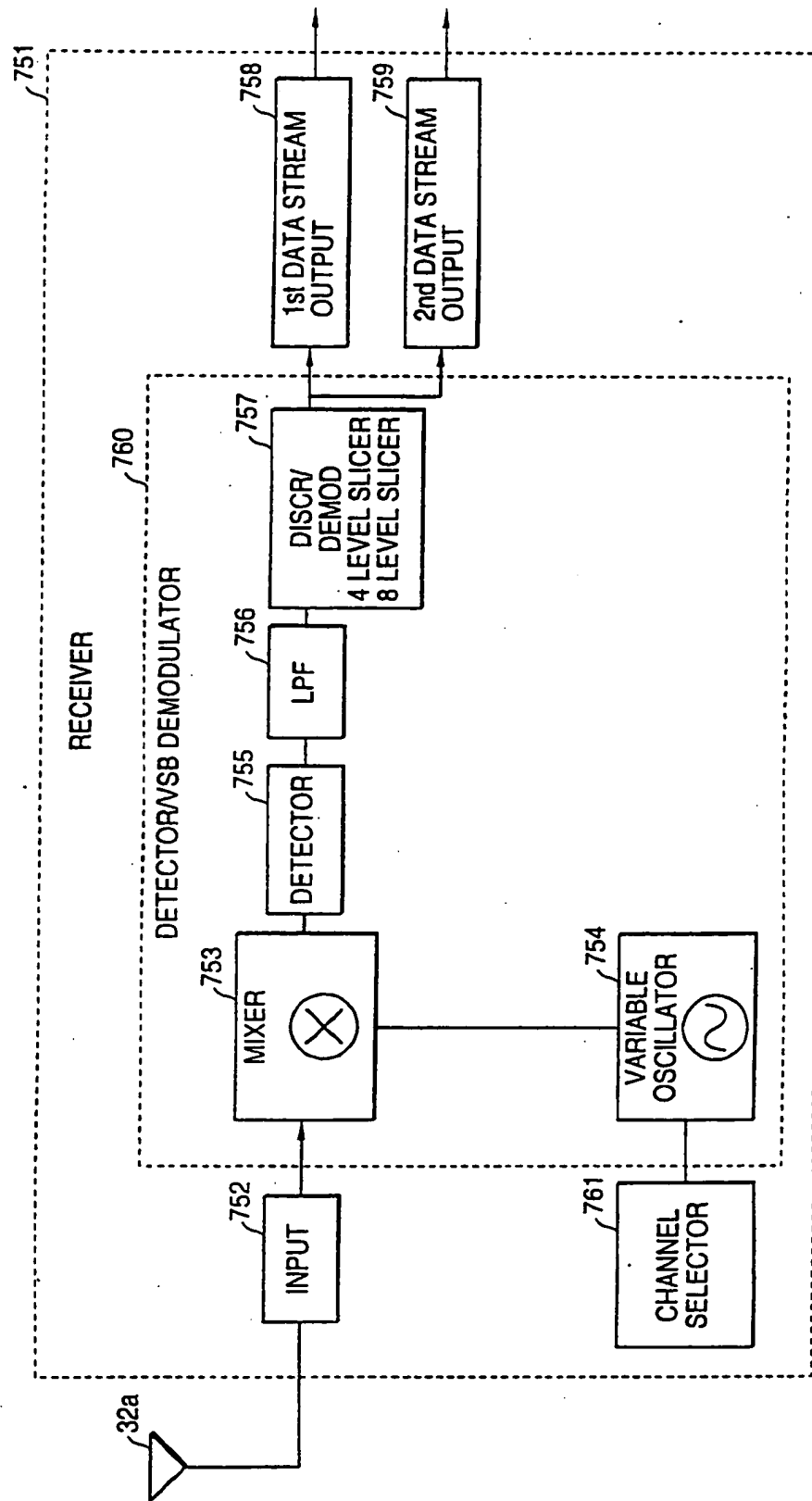


FIG. 64

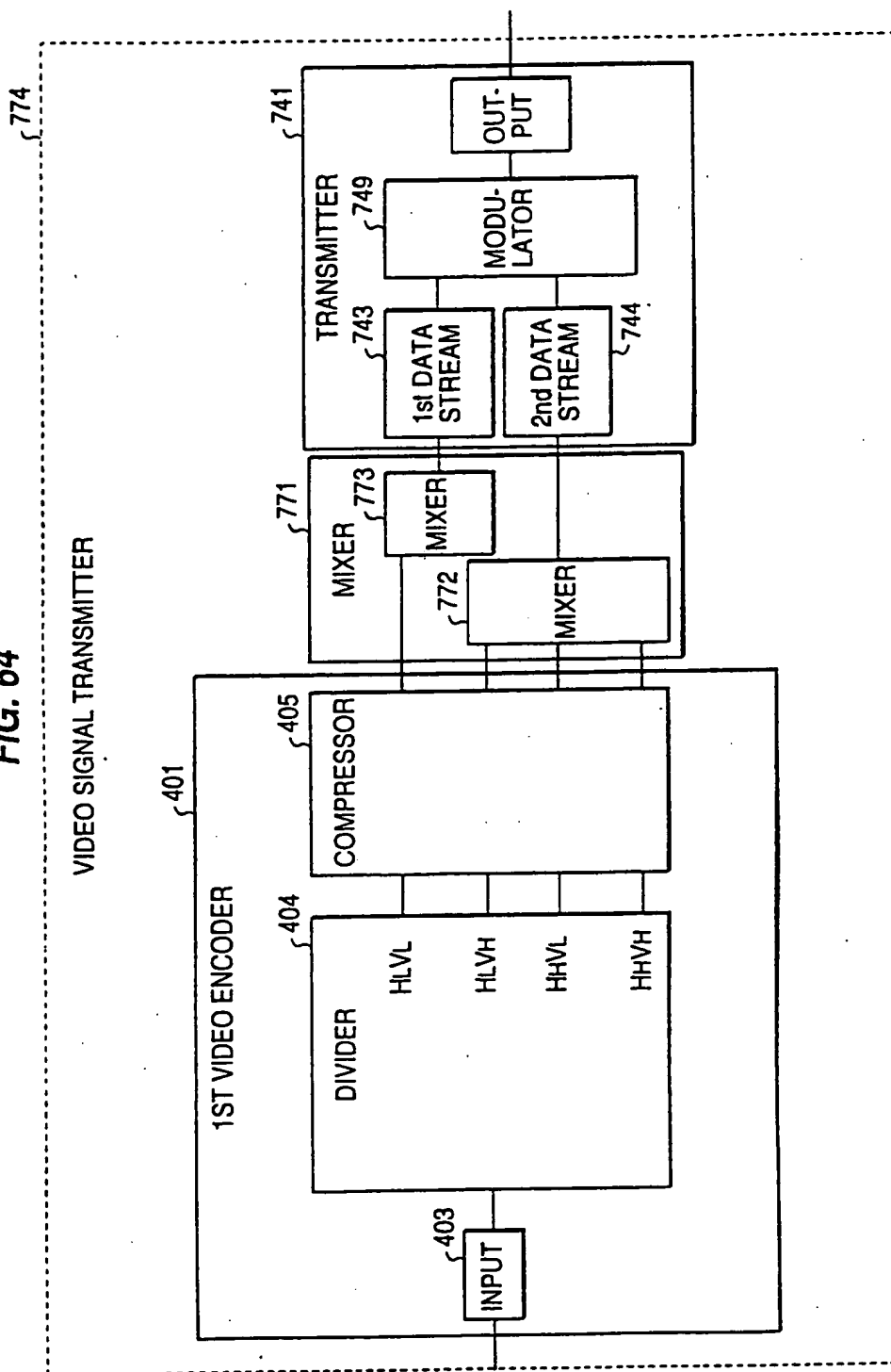


FIG. 65

FIG. 65

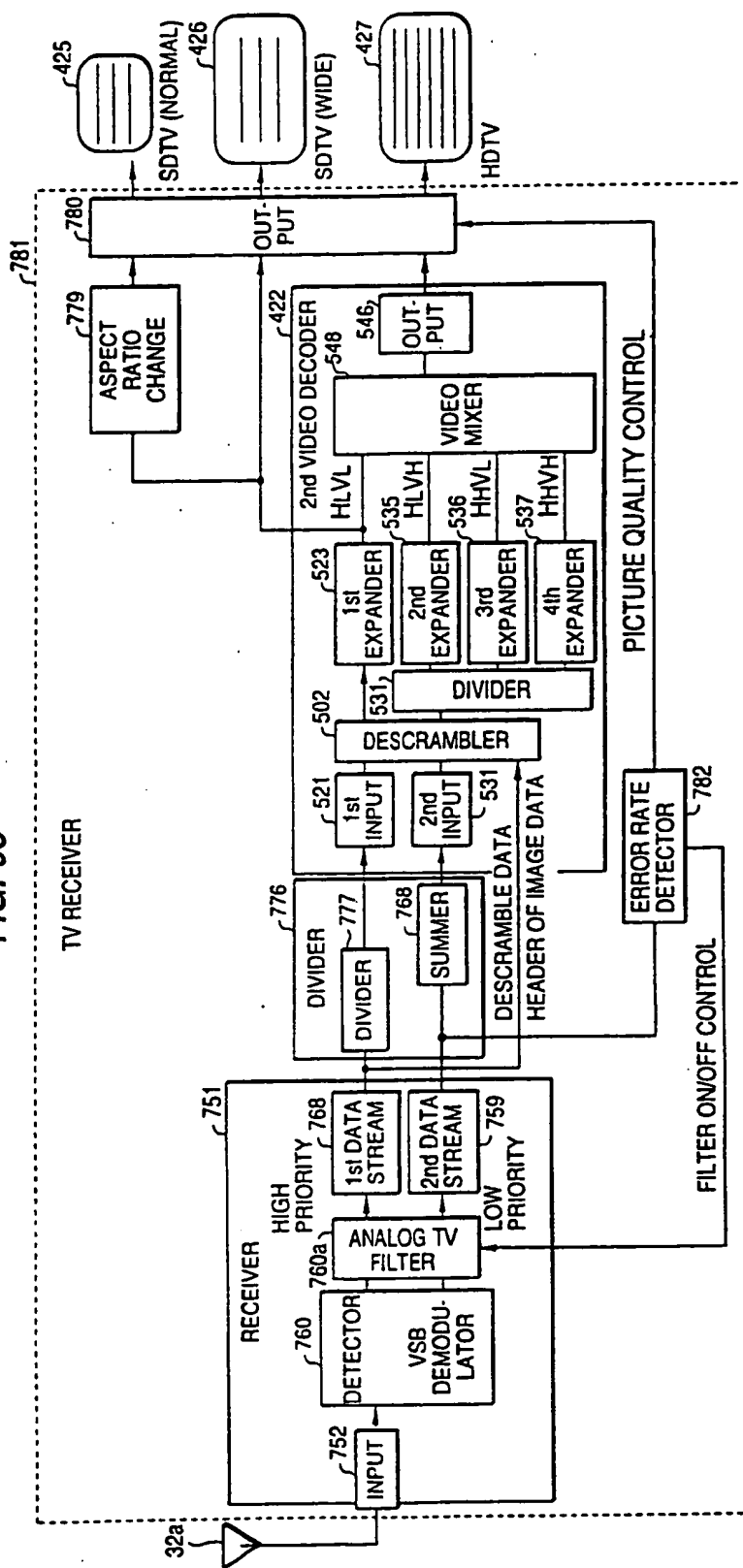
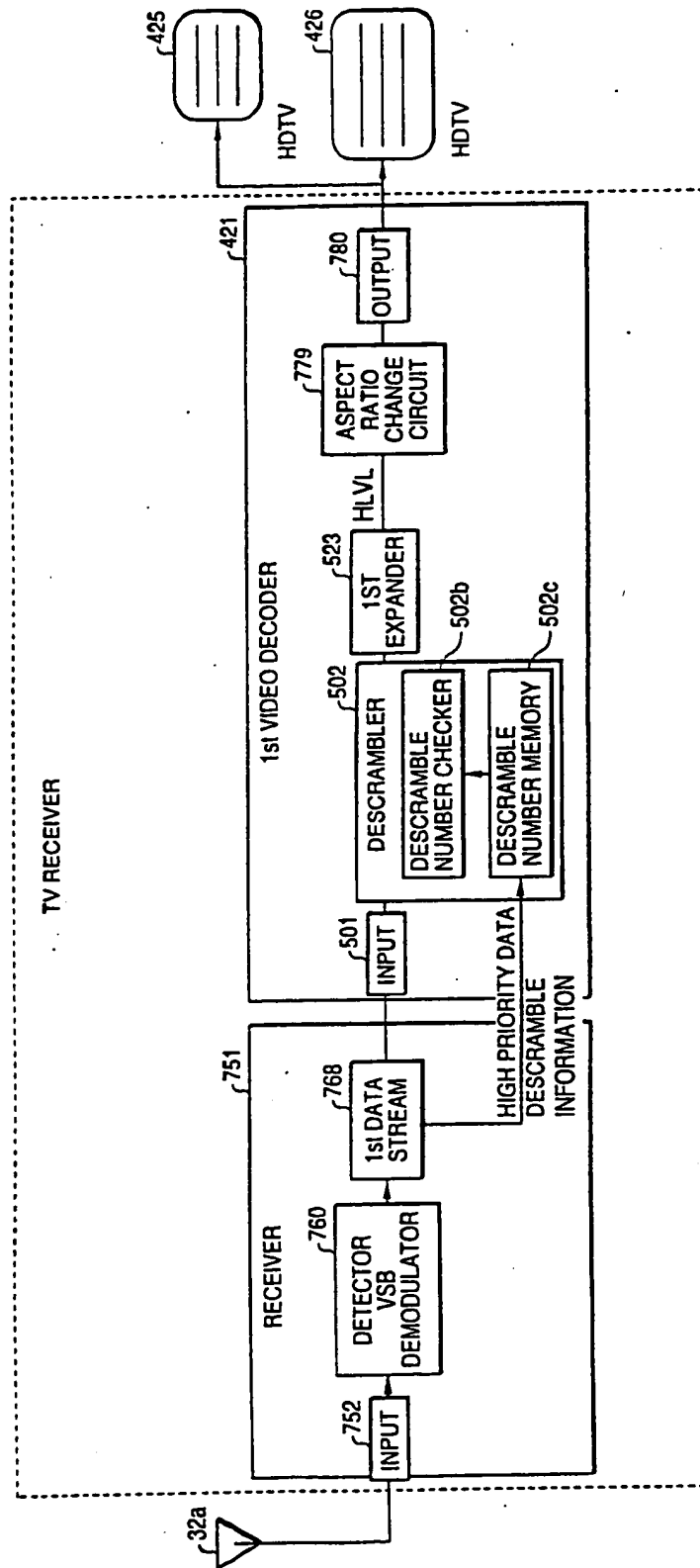
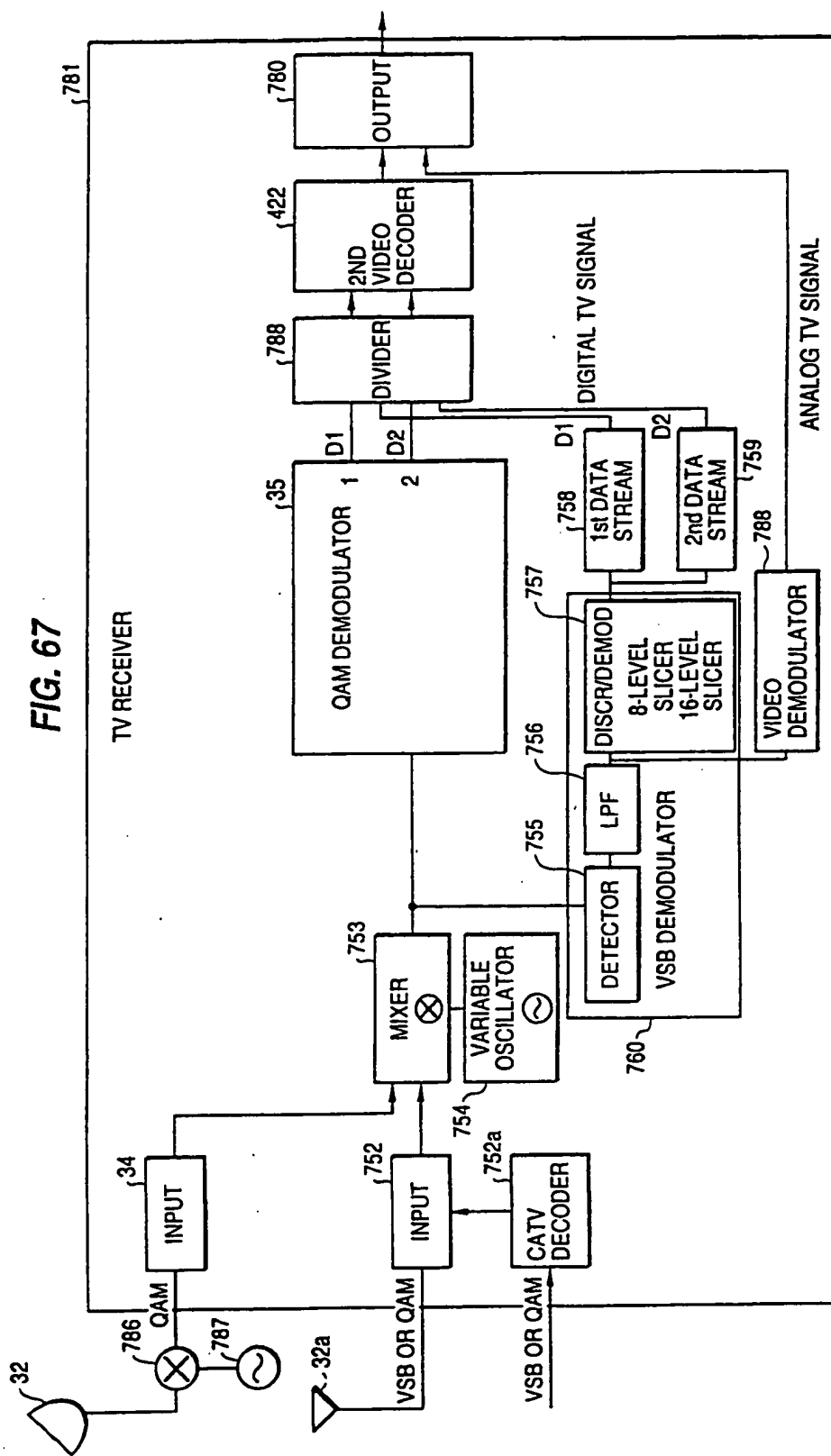


FIG. 66





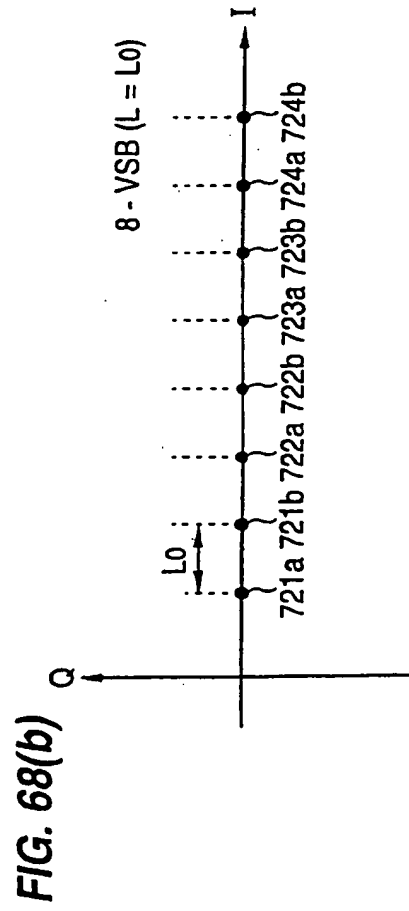
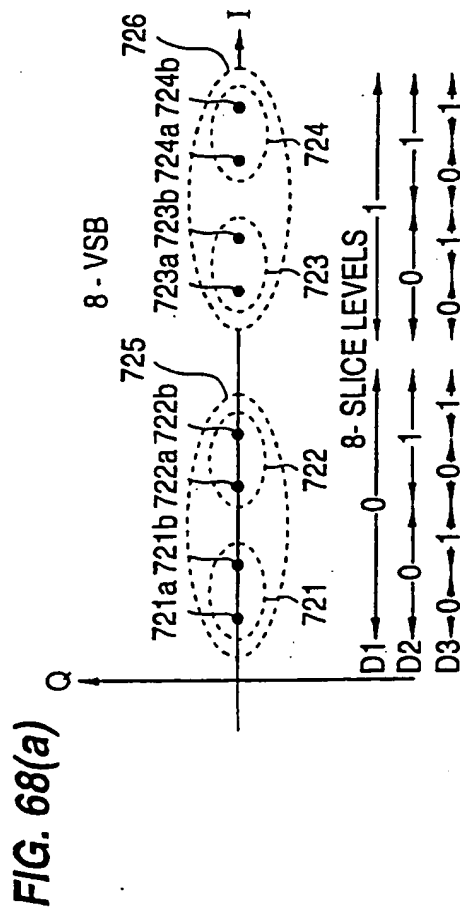


FIG. 68(c)

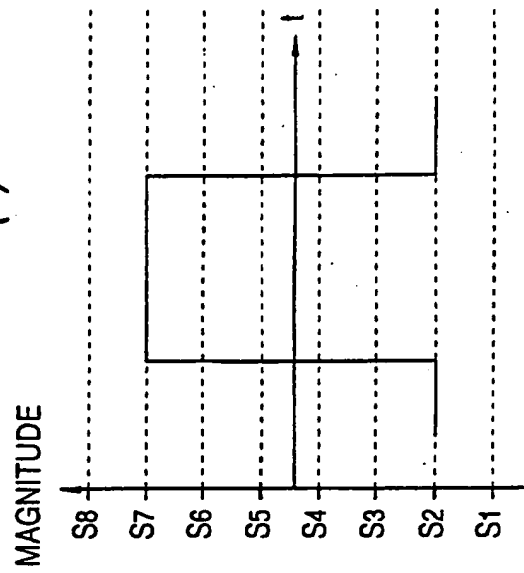


FIG. 69

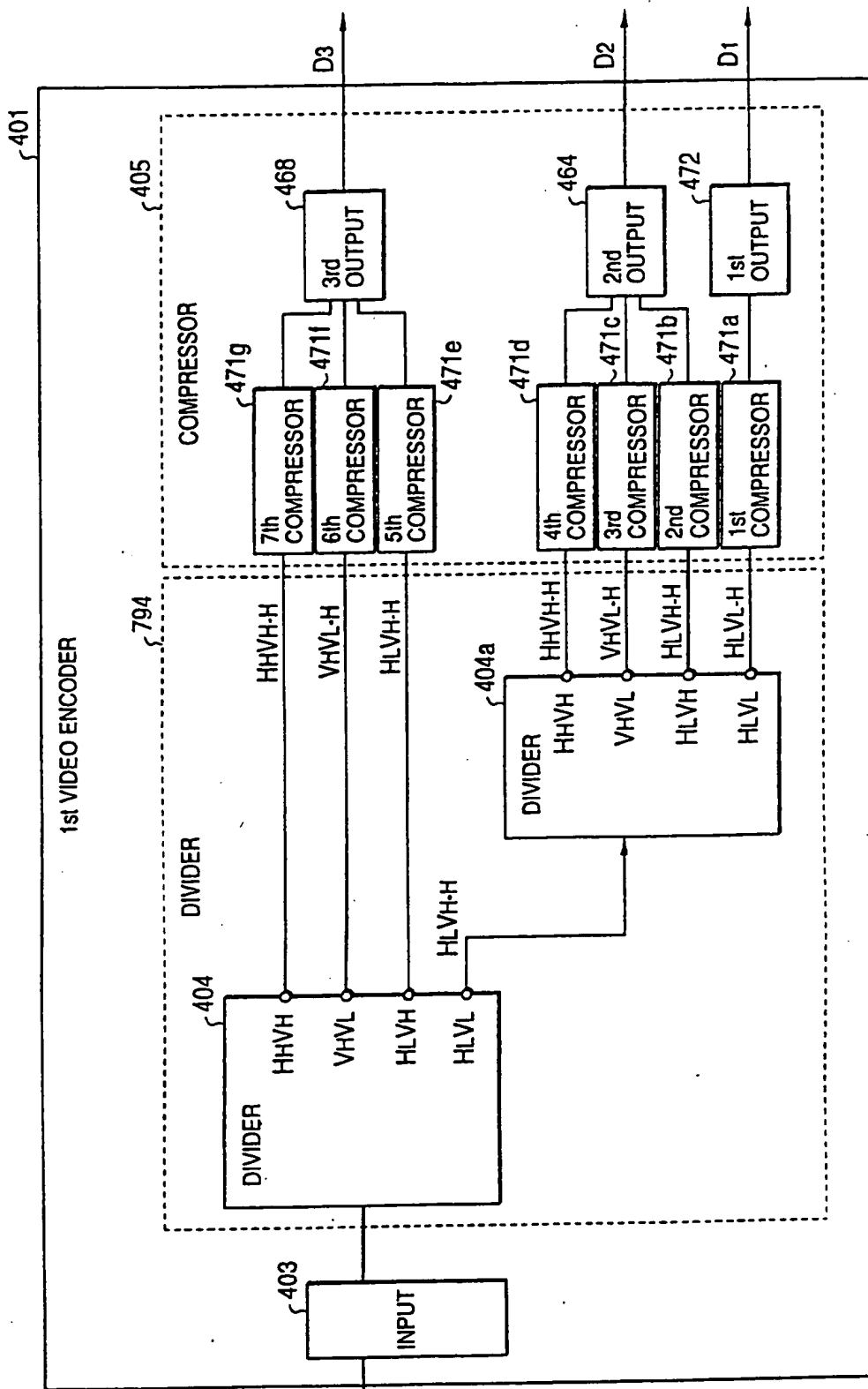


FIG. 70

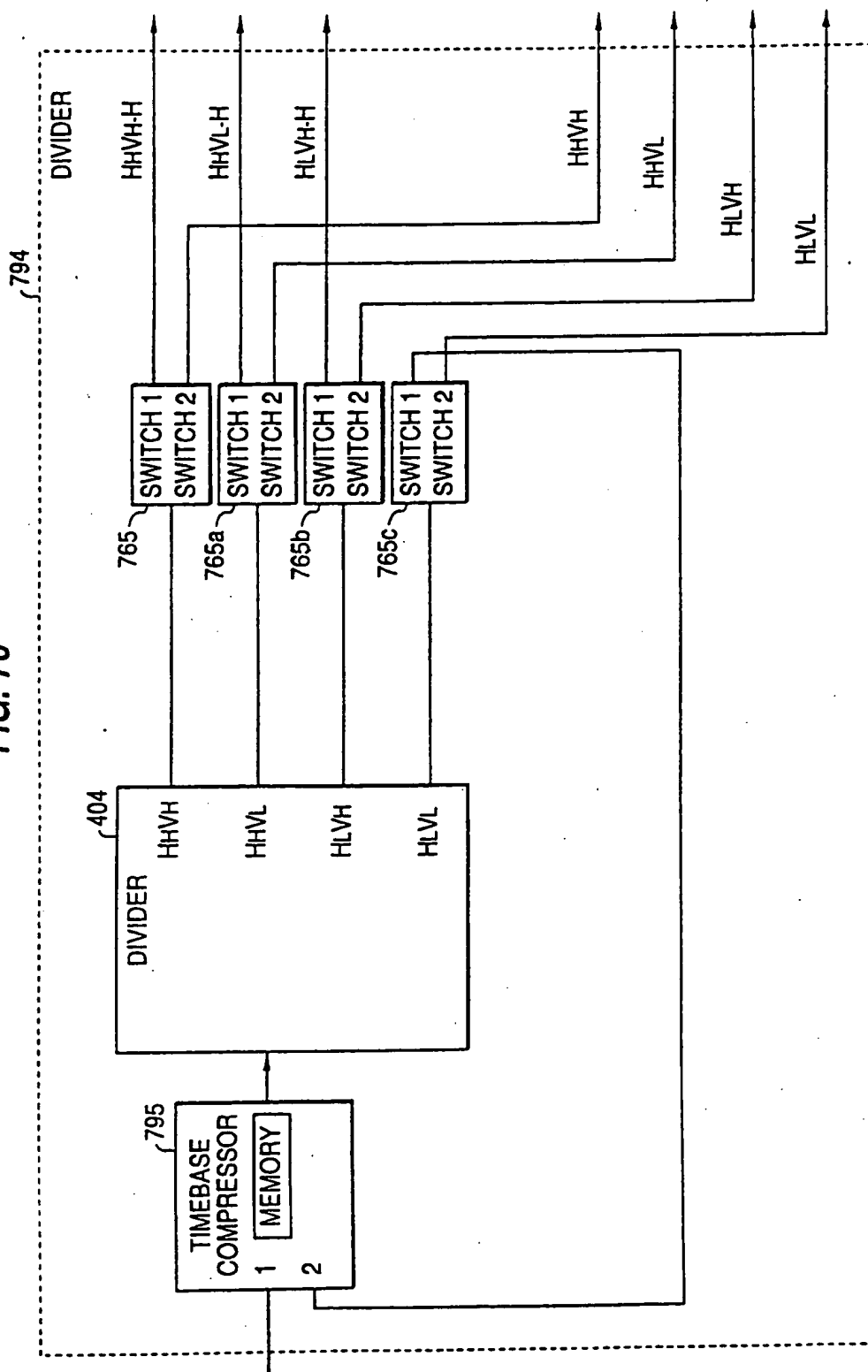


FIG. 71

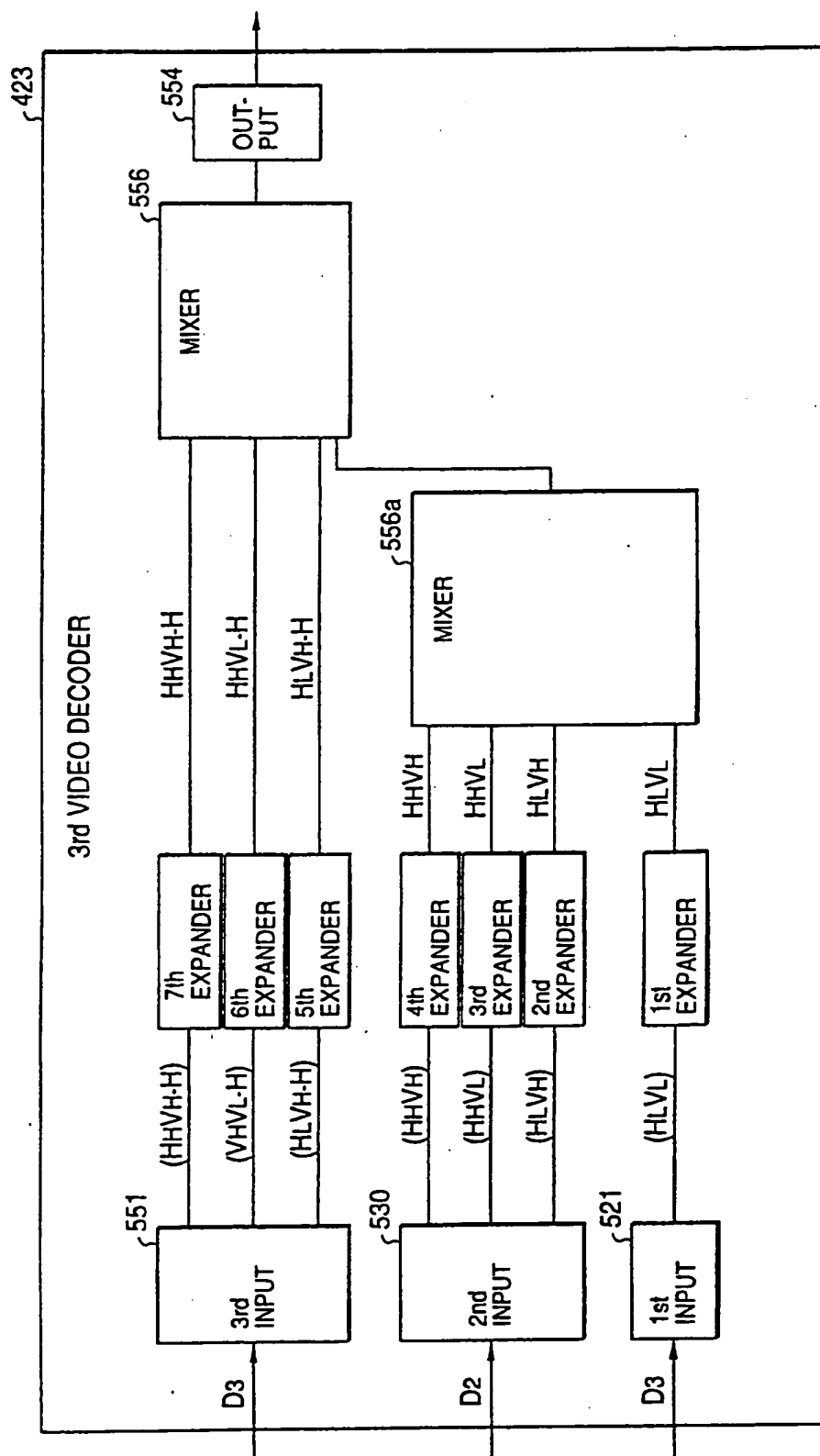


FIG. 72

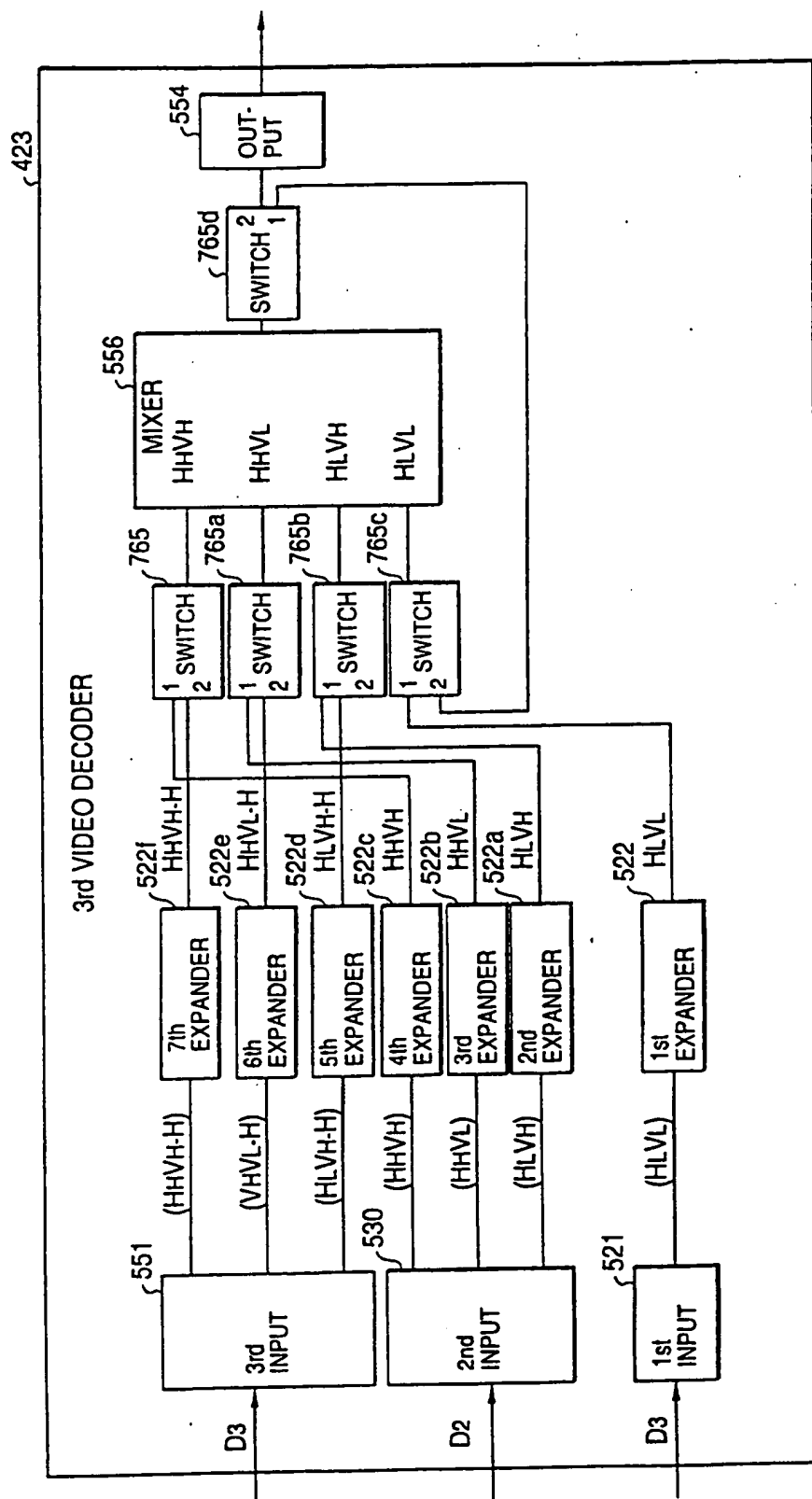


FIG. 73

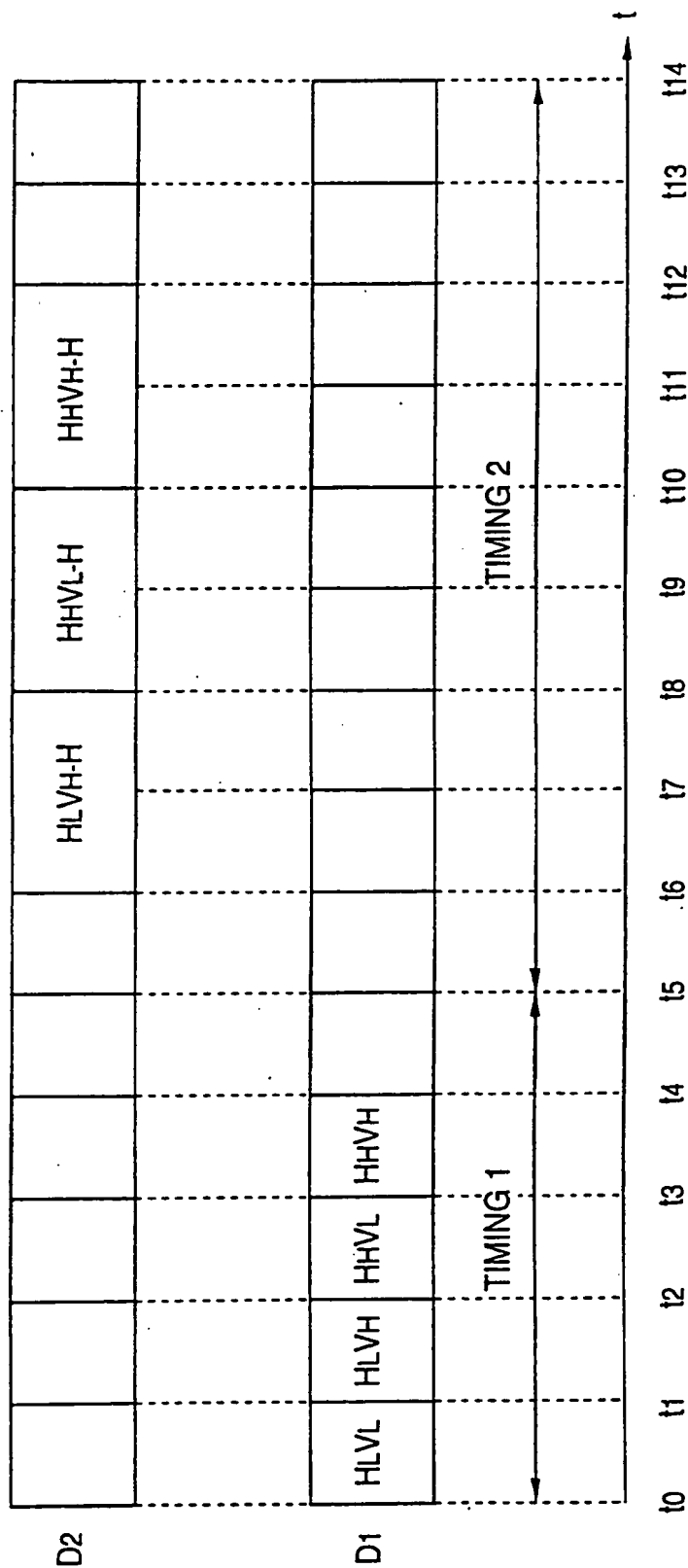


FIG. 74(a)

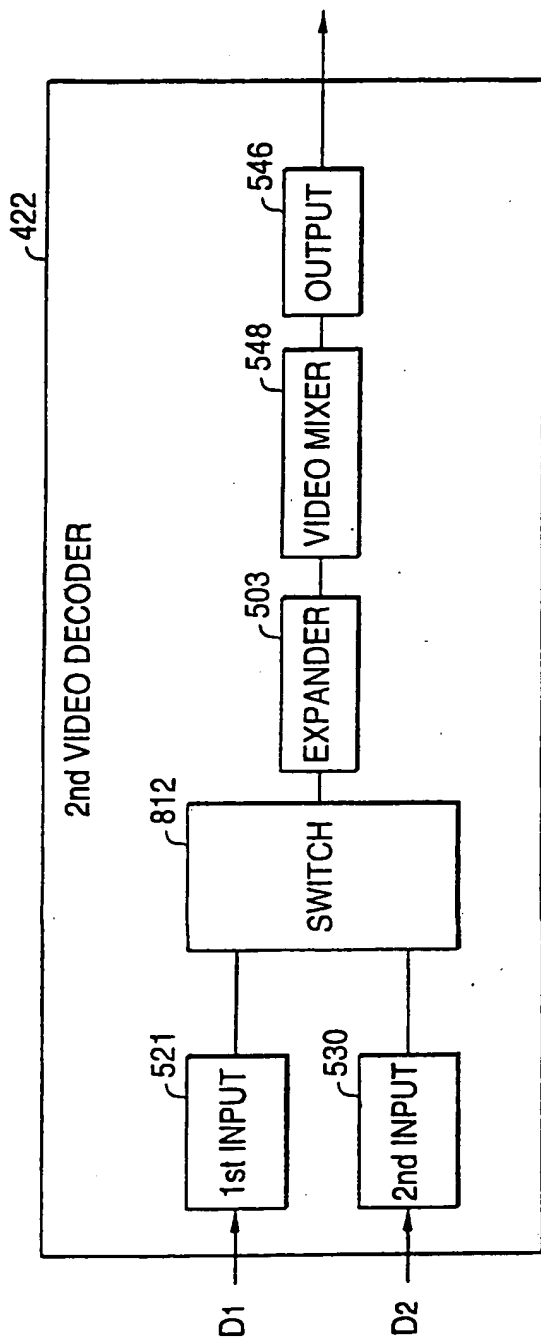
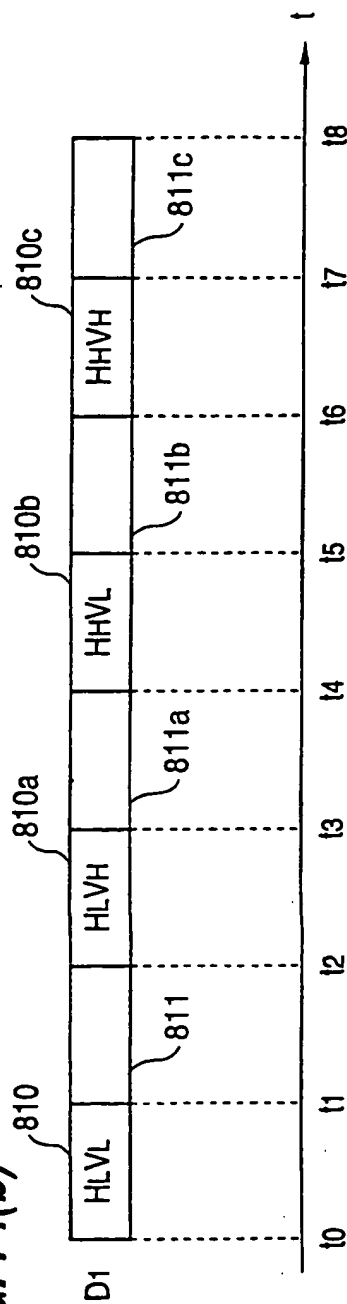


FIG. 74(b)



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FIG. 75

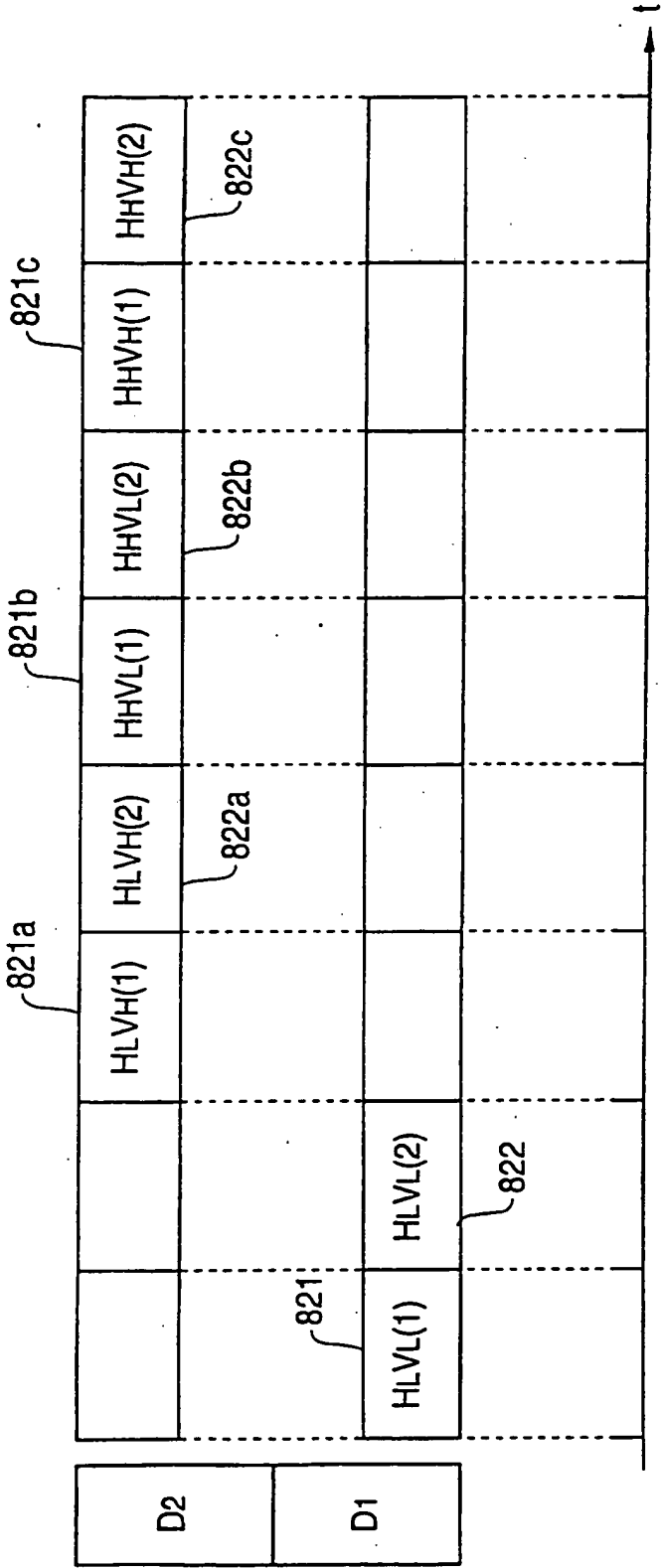


FIG. 76

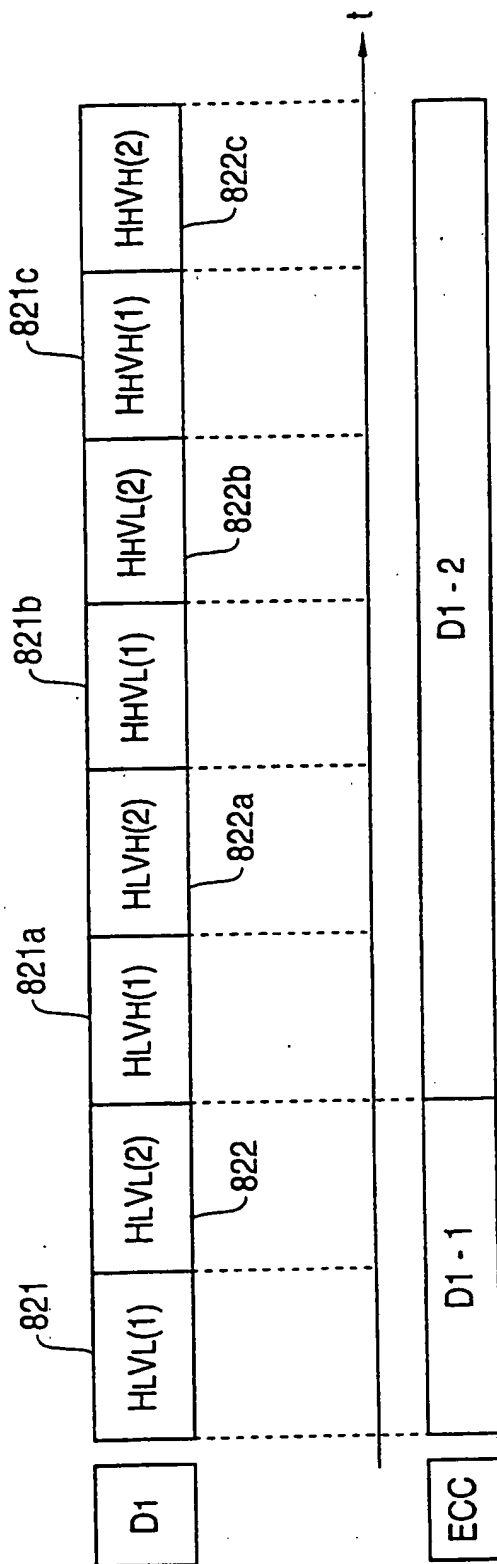


FIG. 78

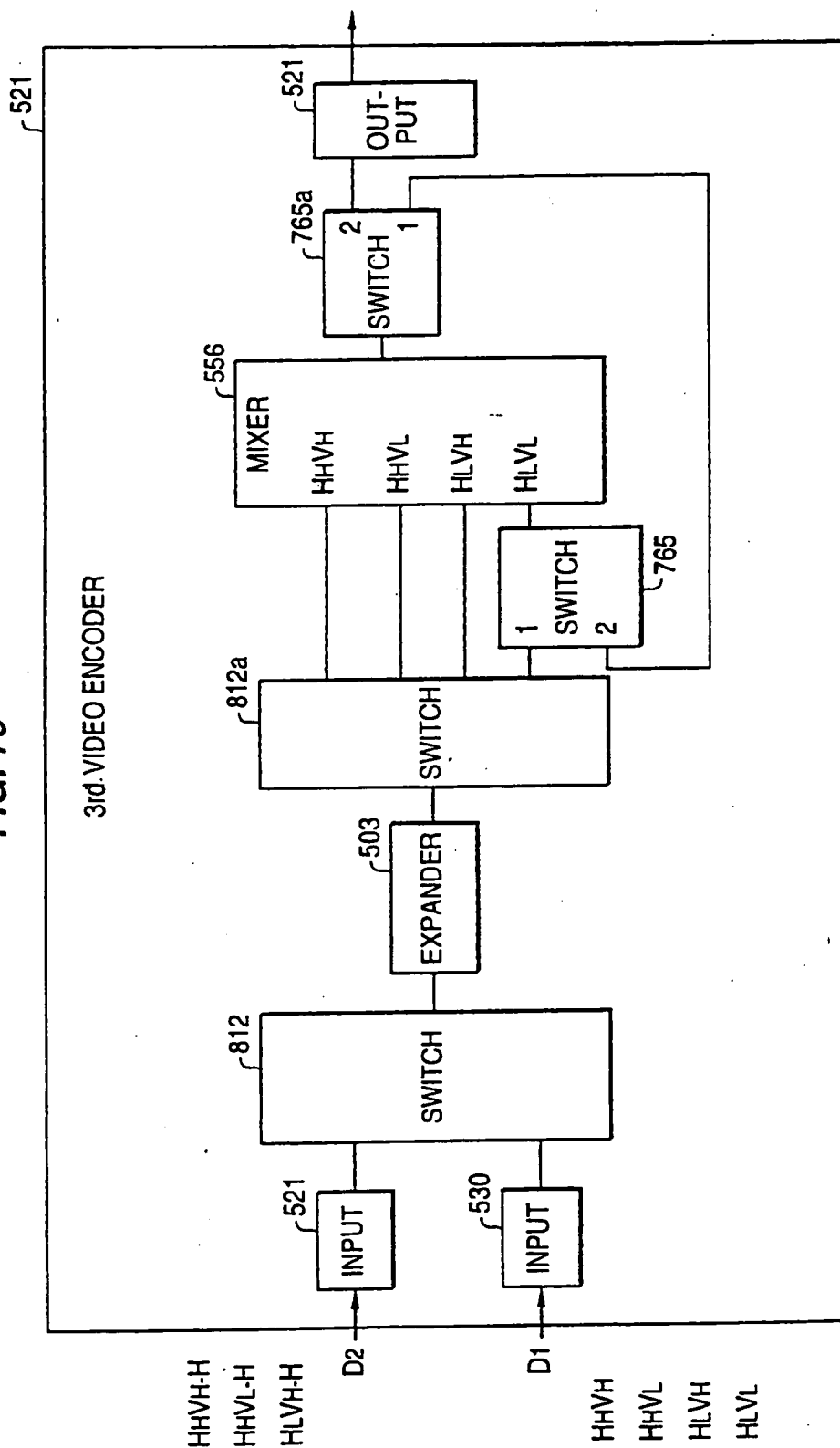


FIG. 79

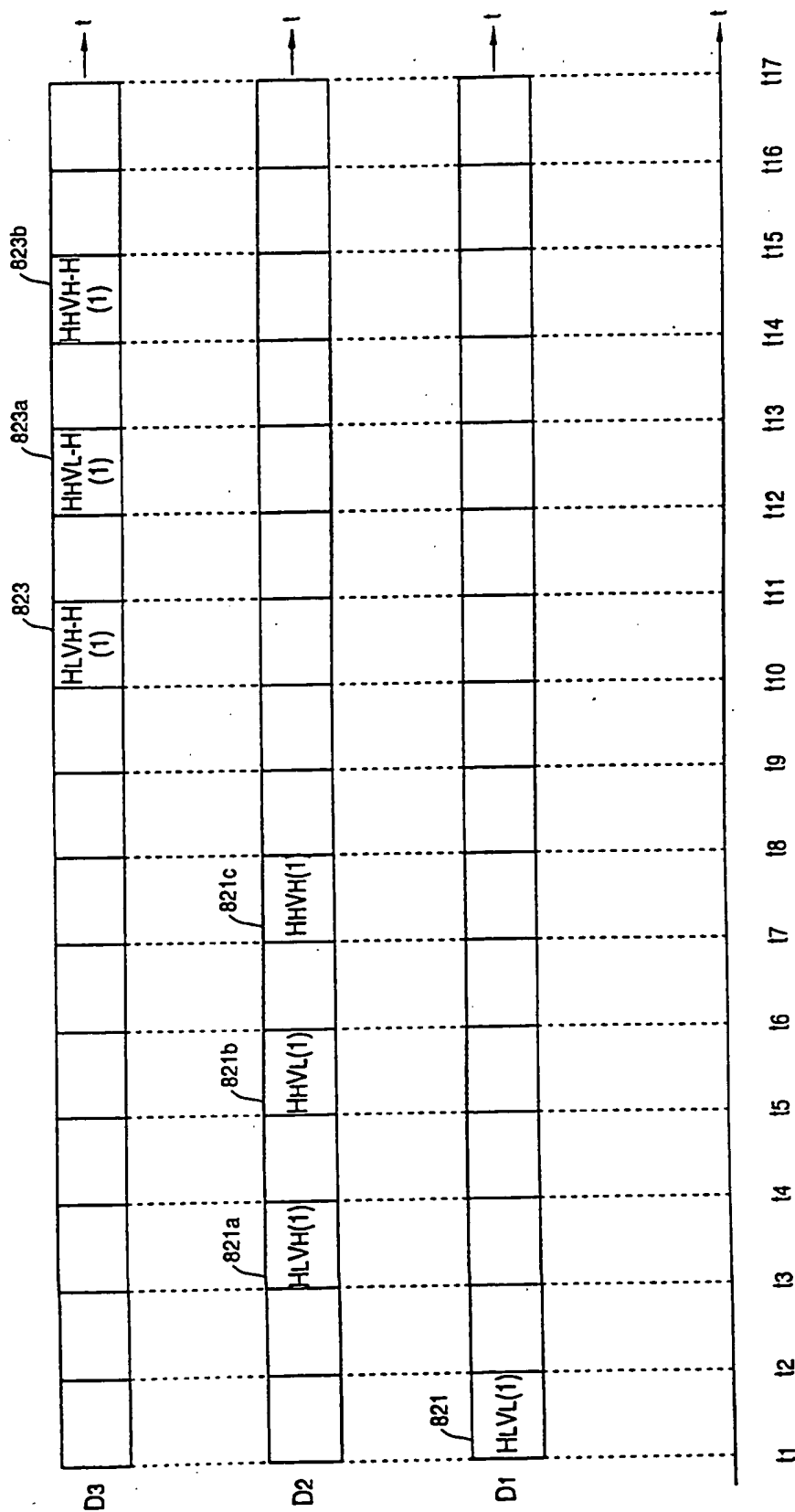


FIG. 80

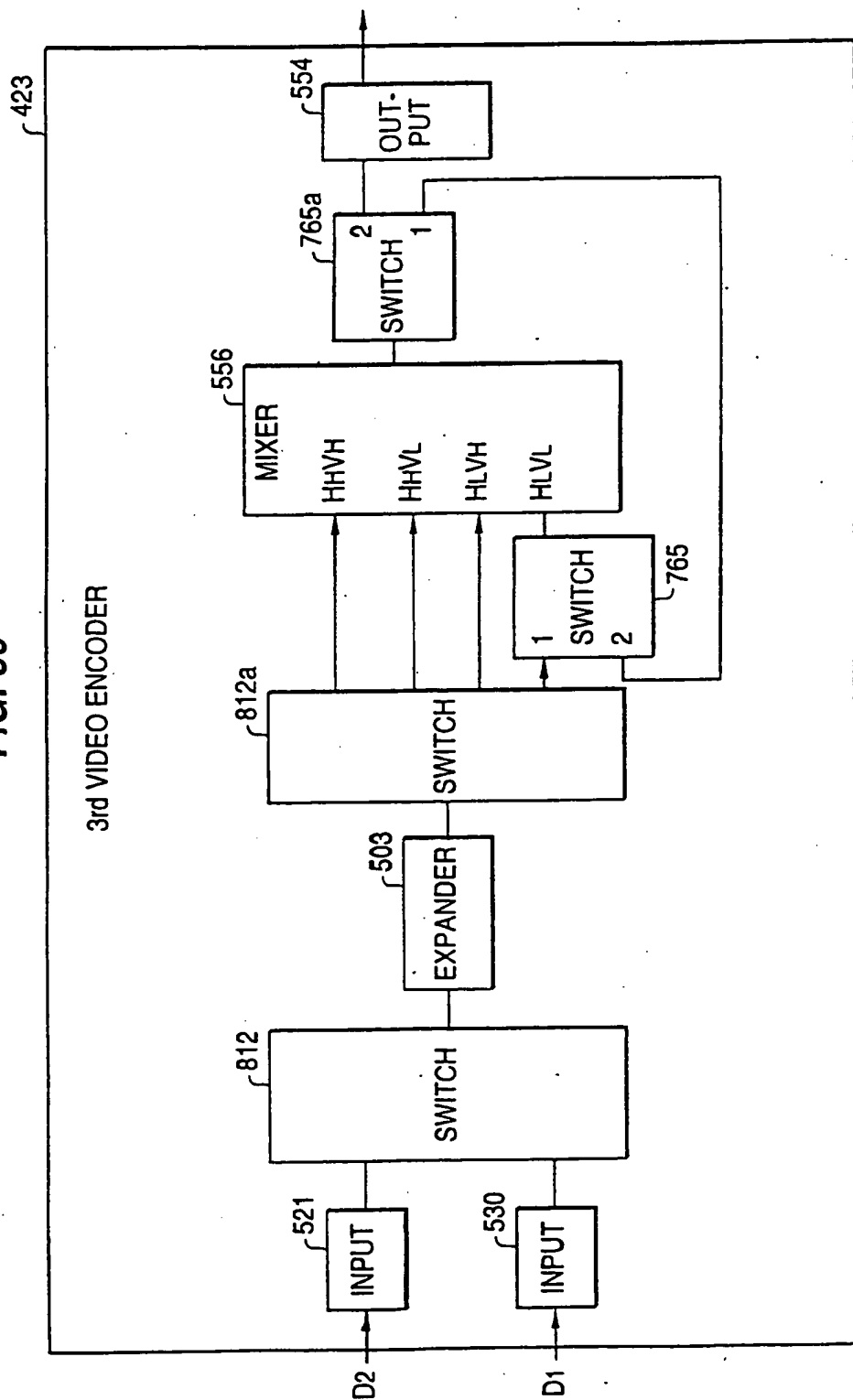
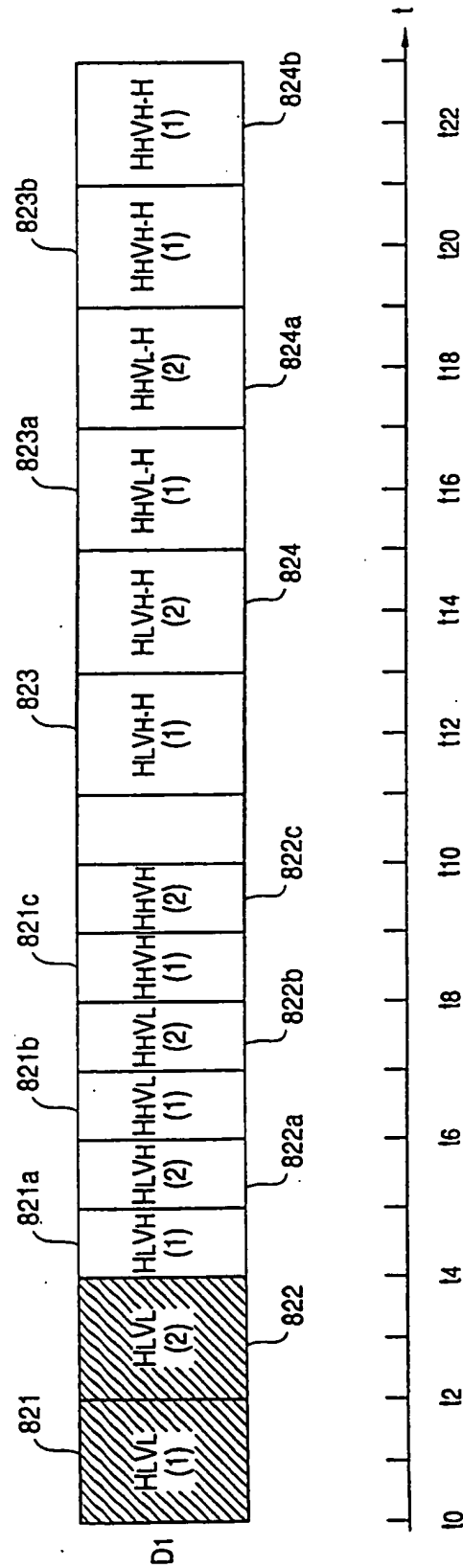


FIG. 81



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FIG. 82

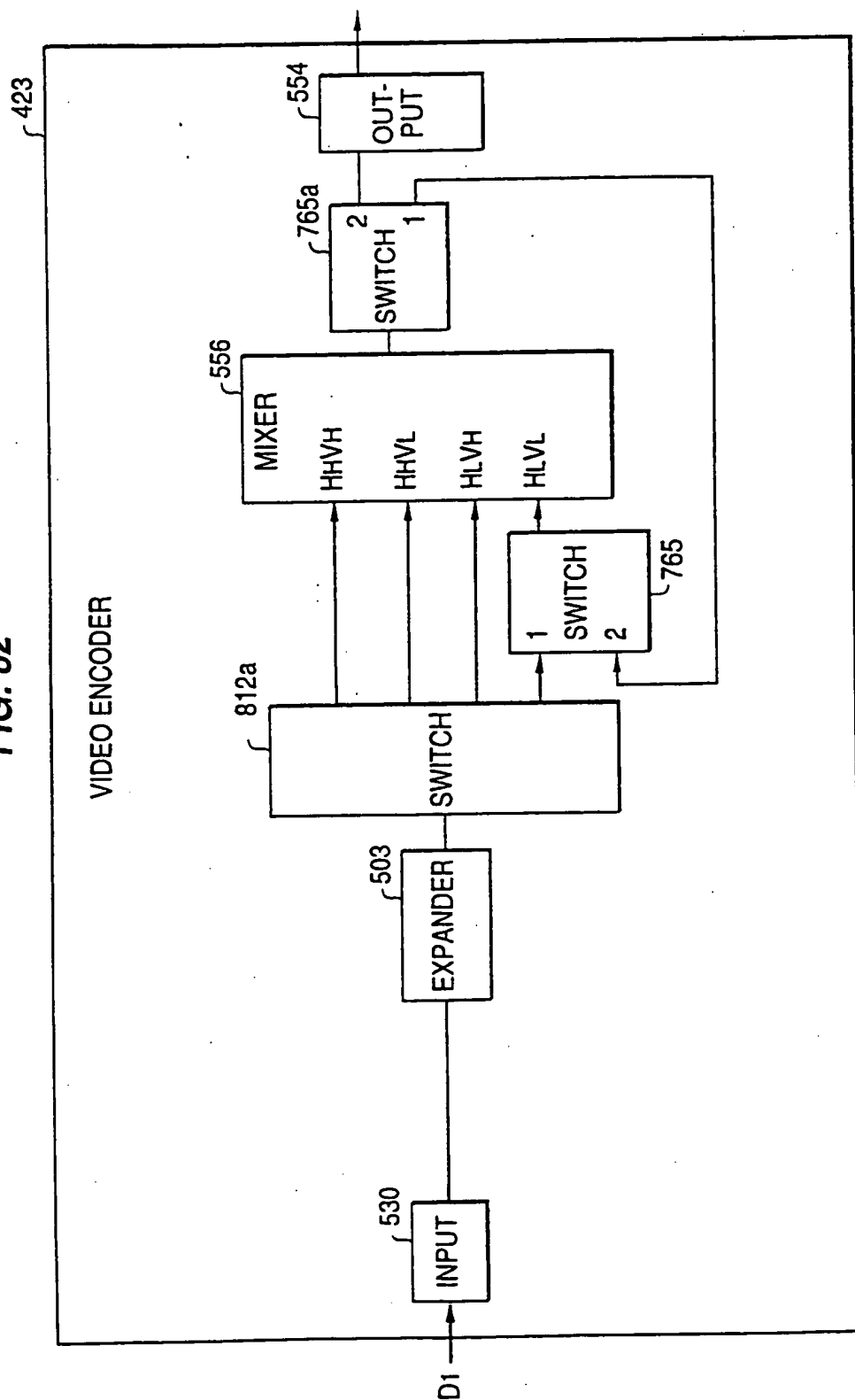


FIG. 83

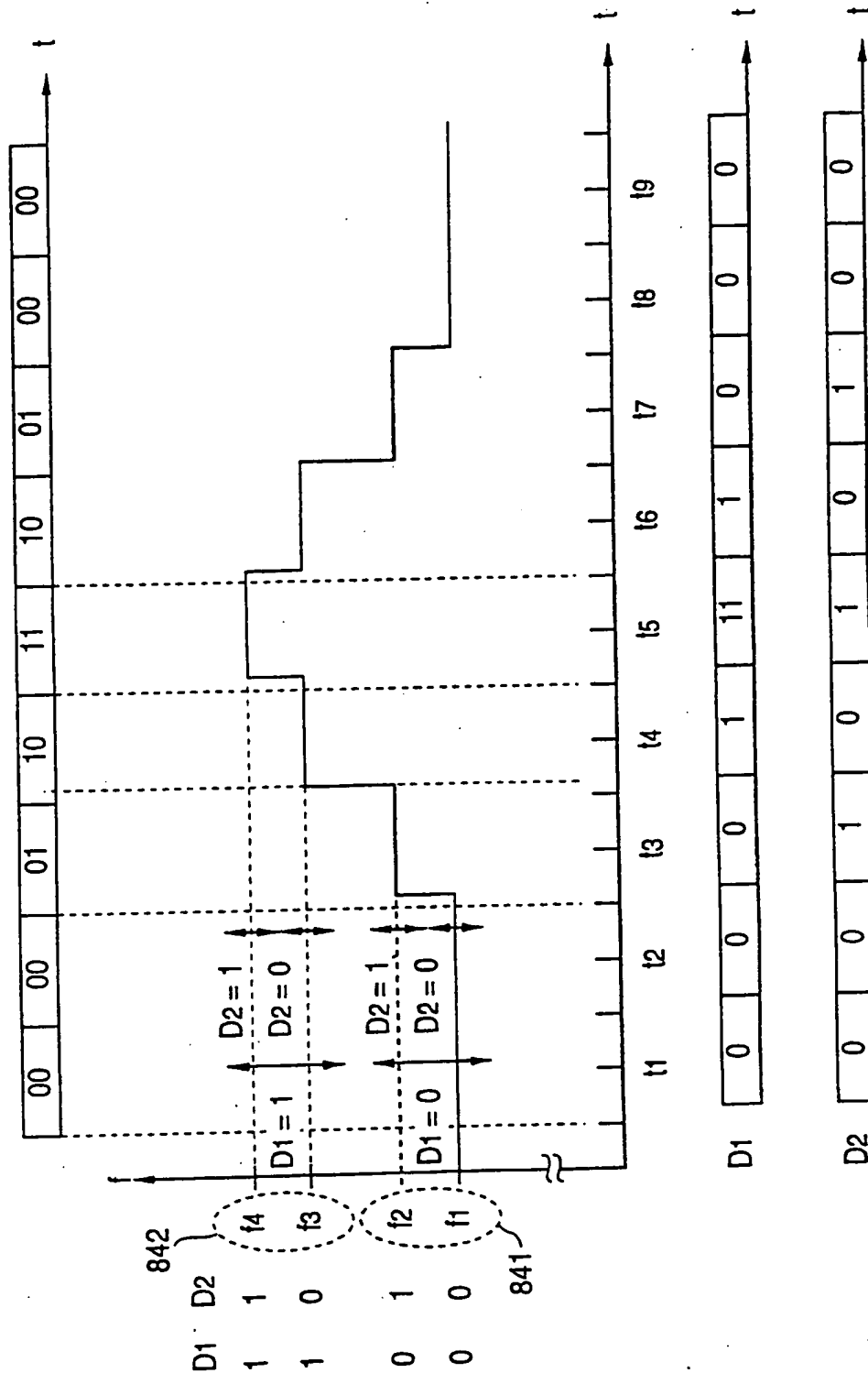


FIG. 84

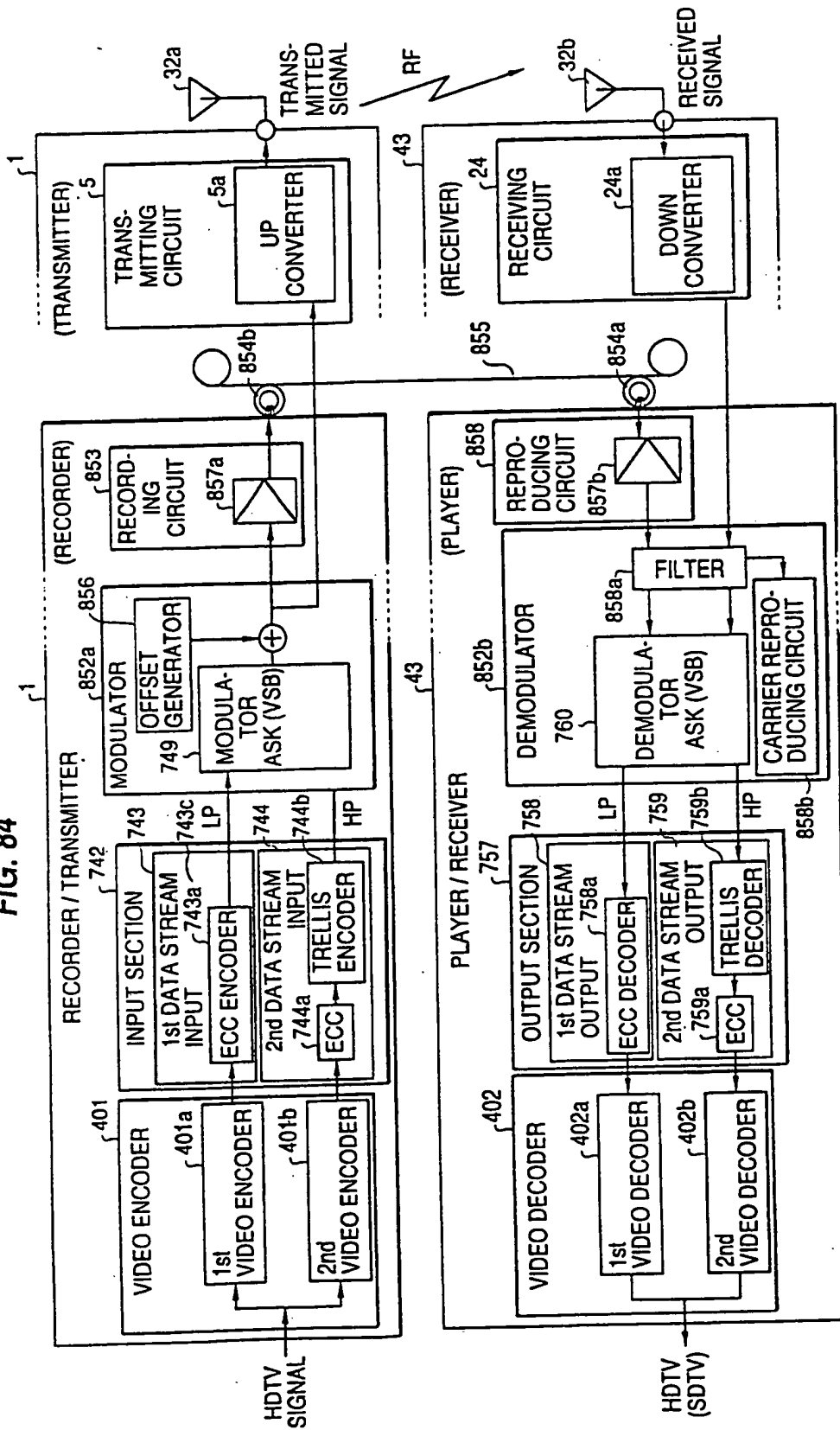


FIG. 85

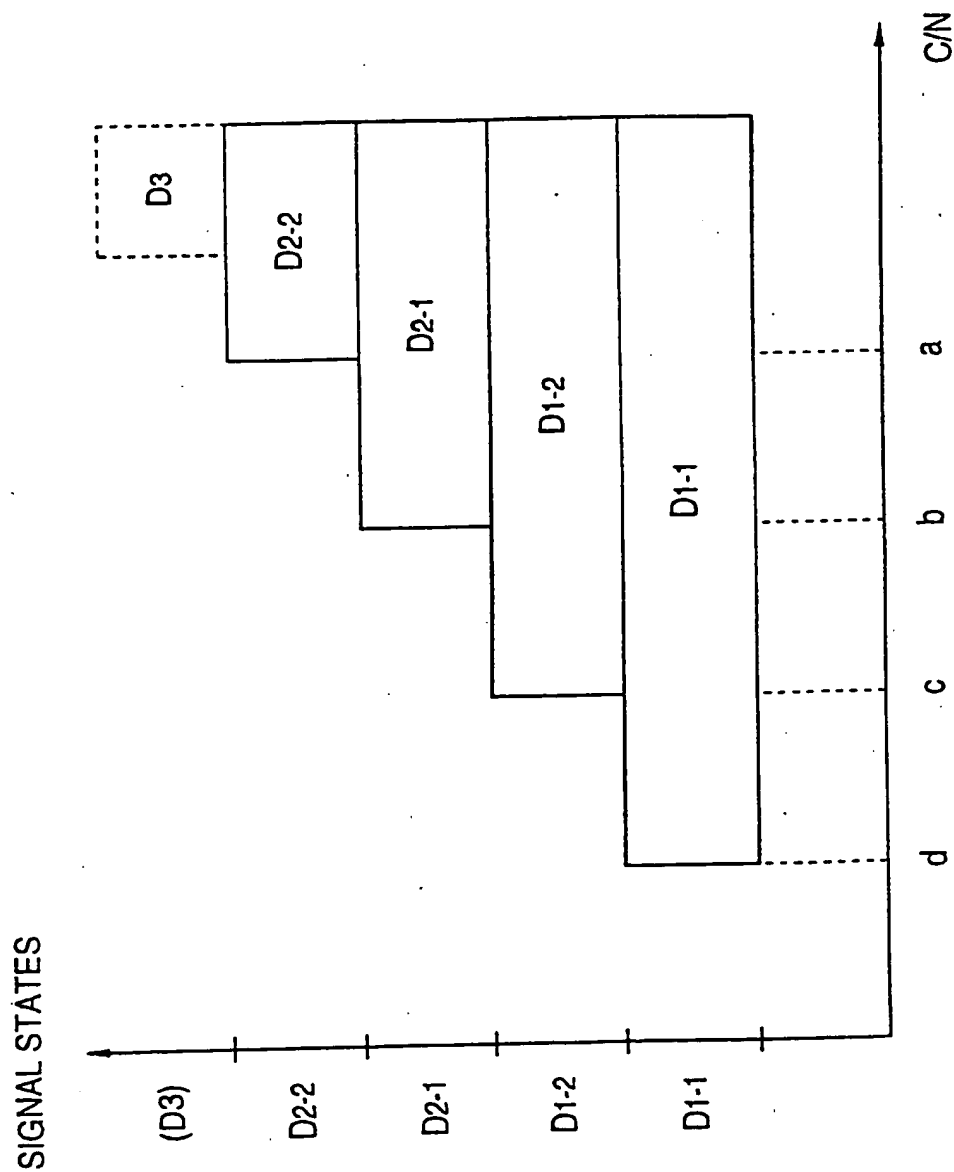
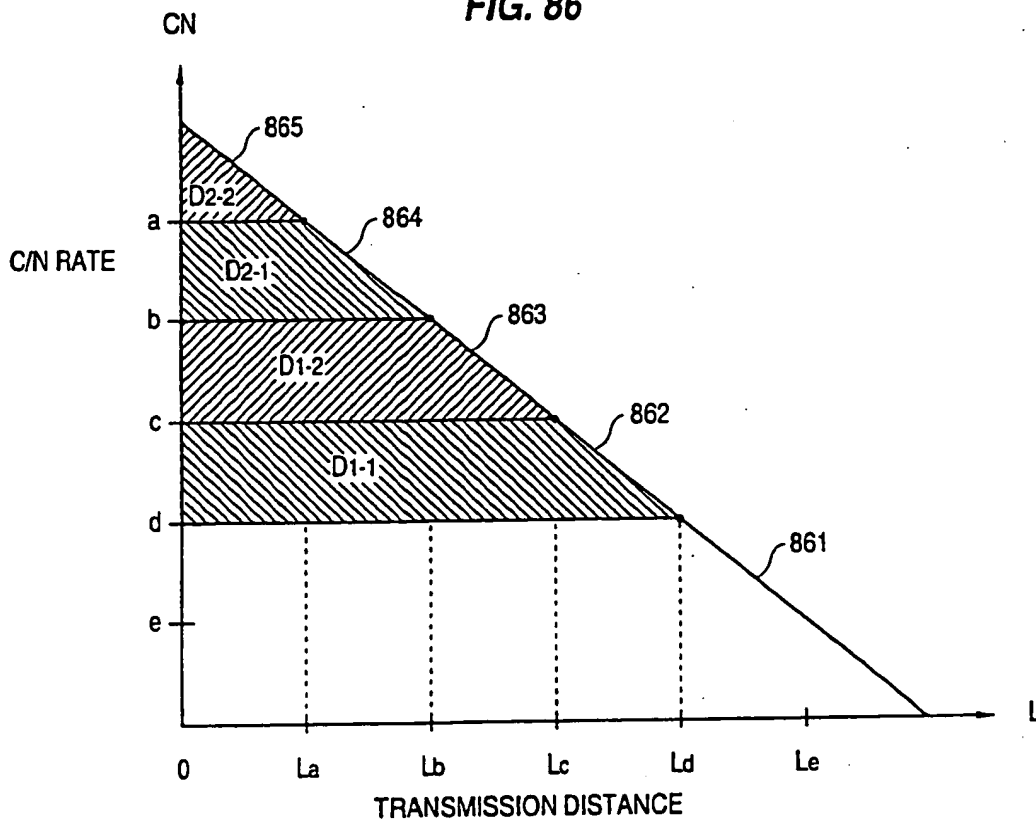
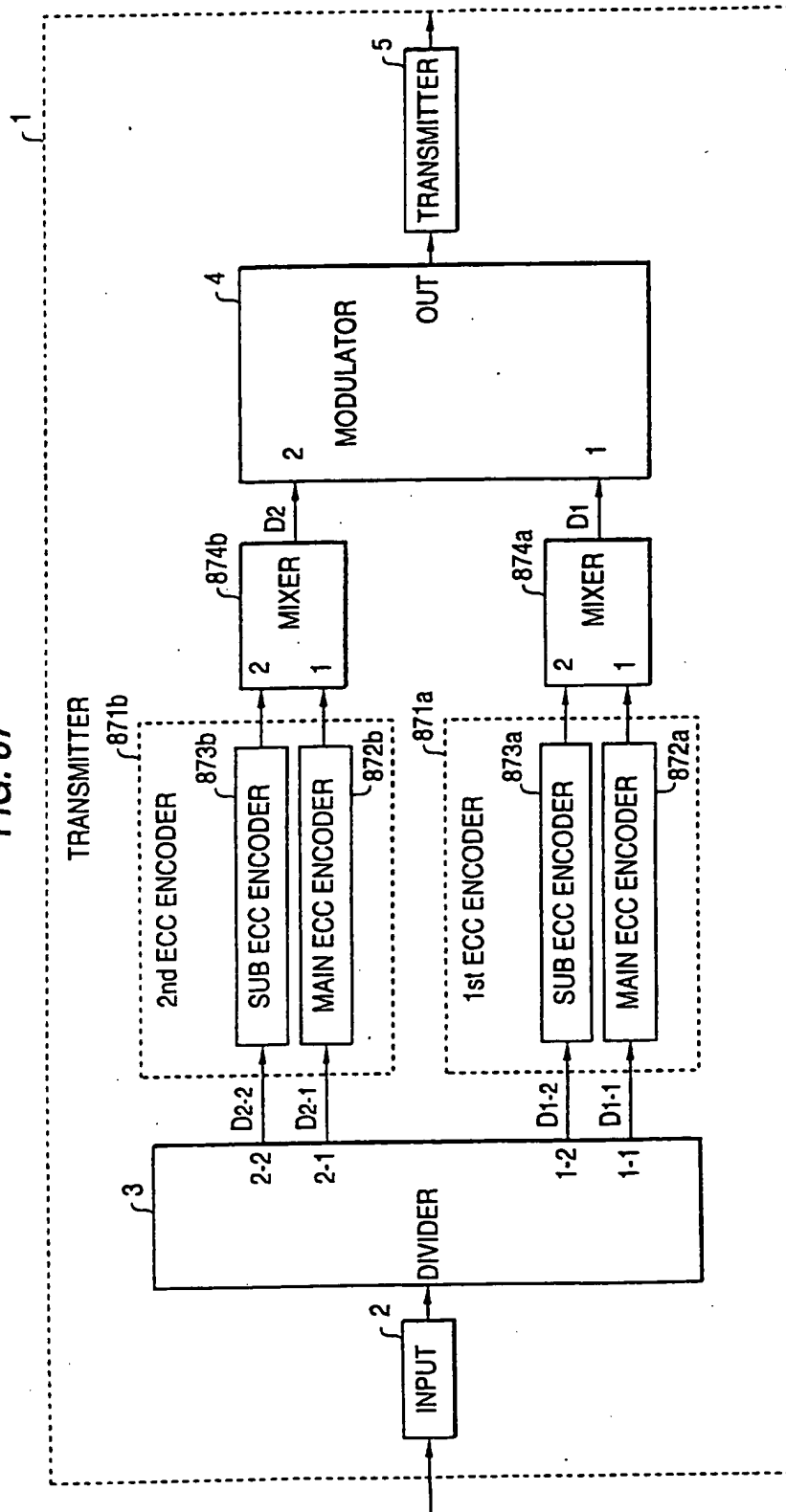


FIG. 86



09660177-1006000

FIG. 87



005001/2709360

FIG. 88

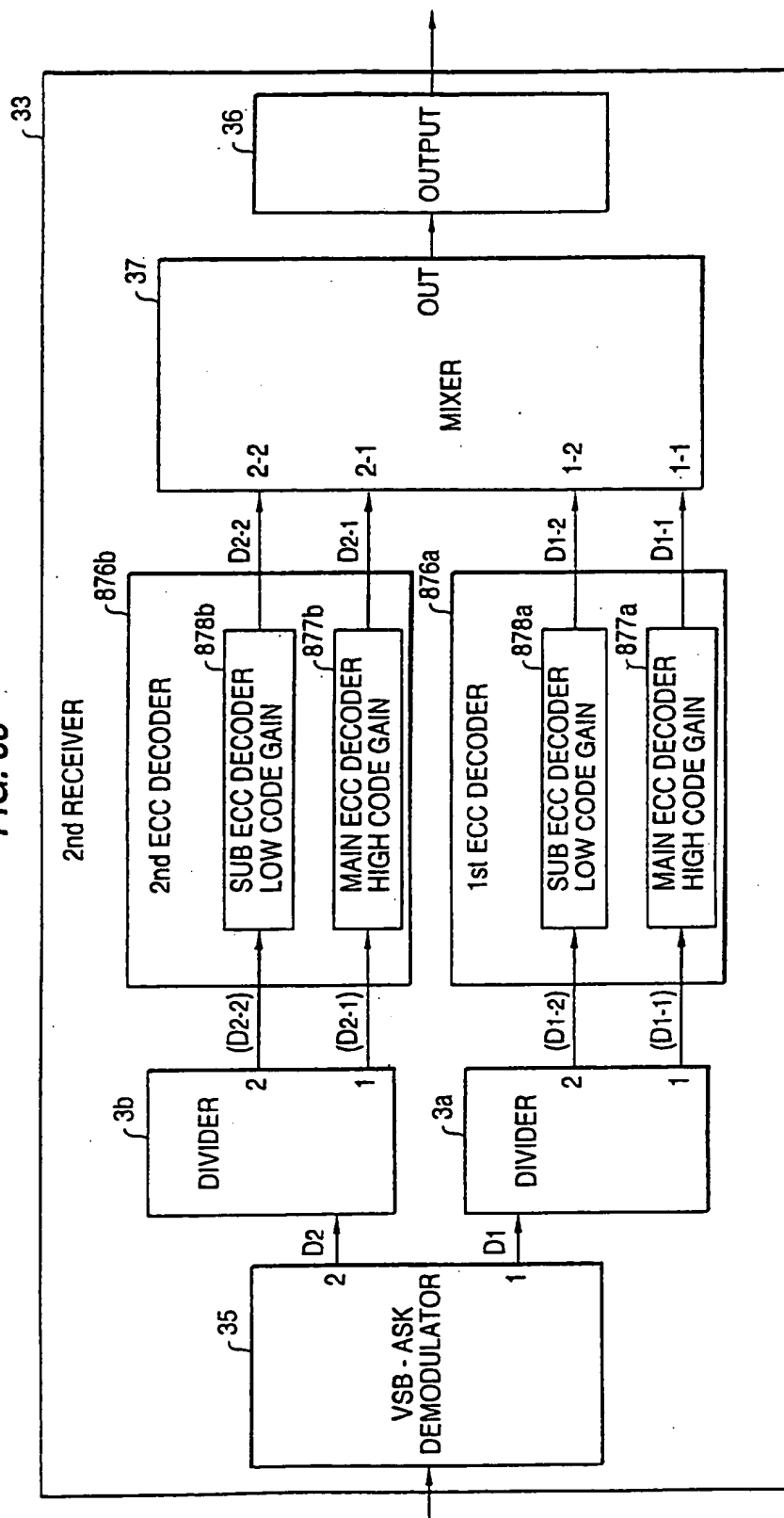
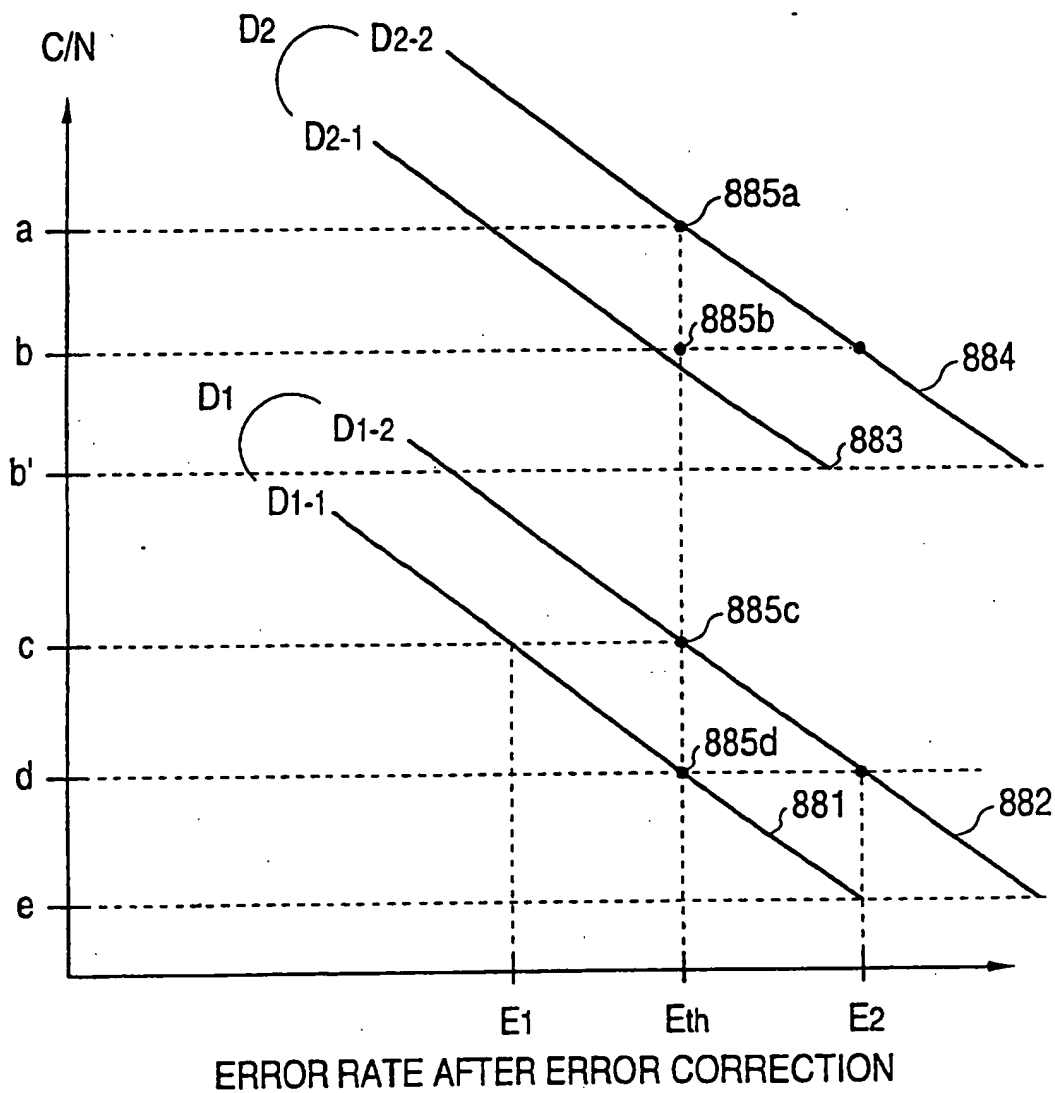


FIG. 89



005007 2/03950

FIG. 90

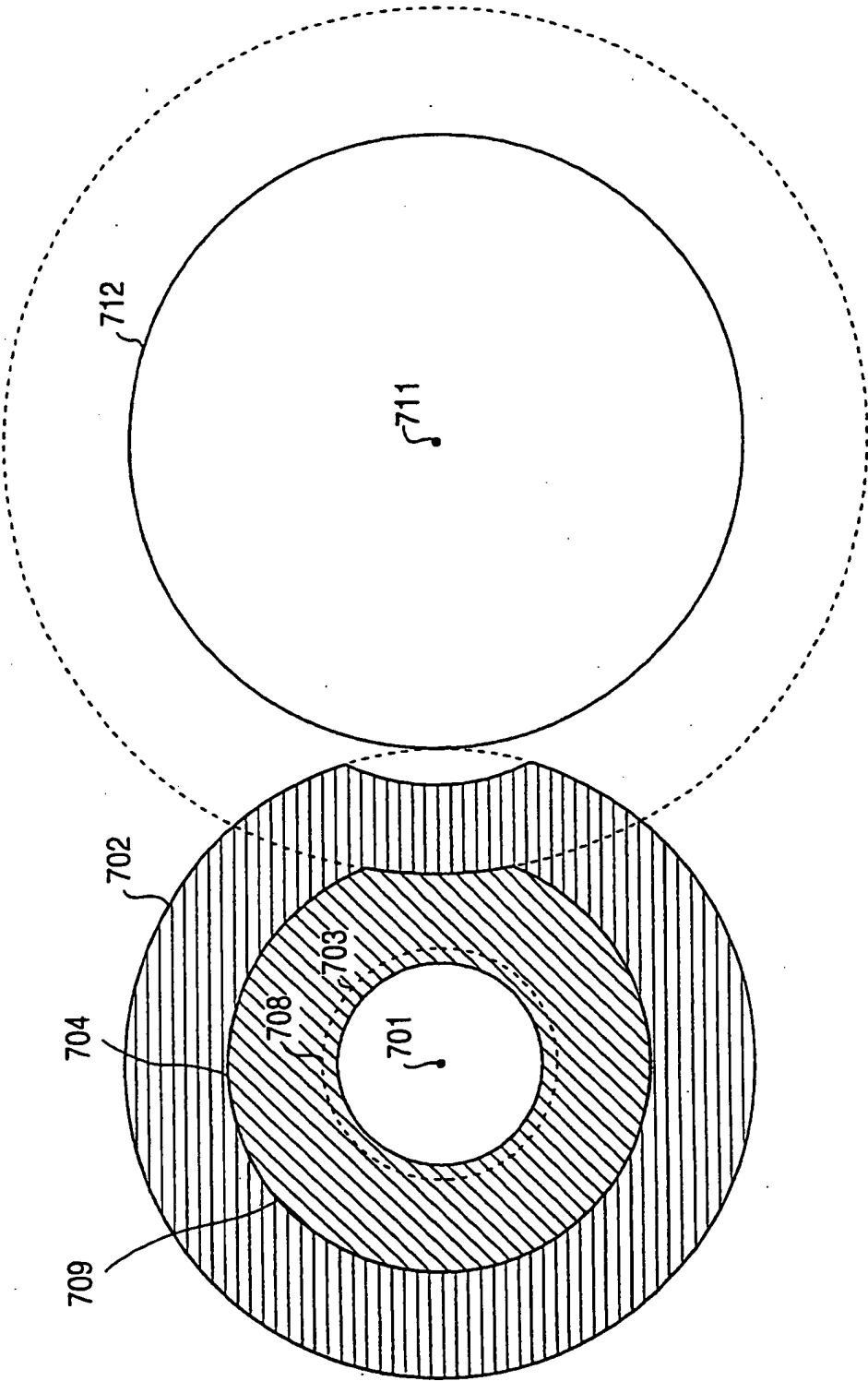
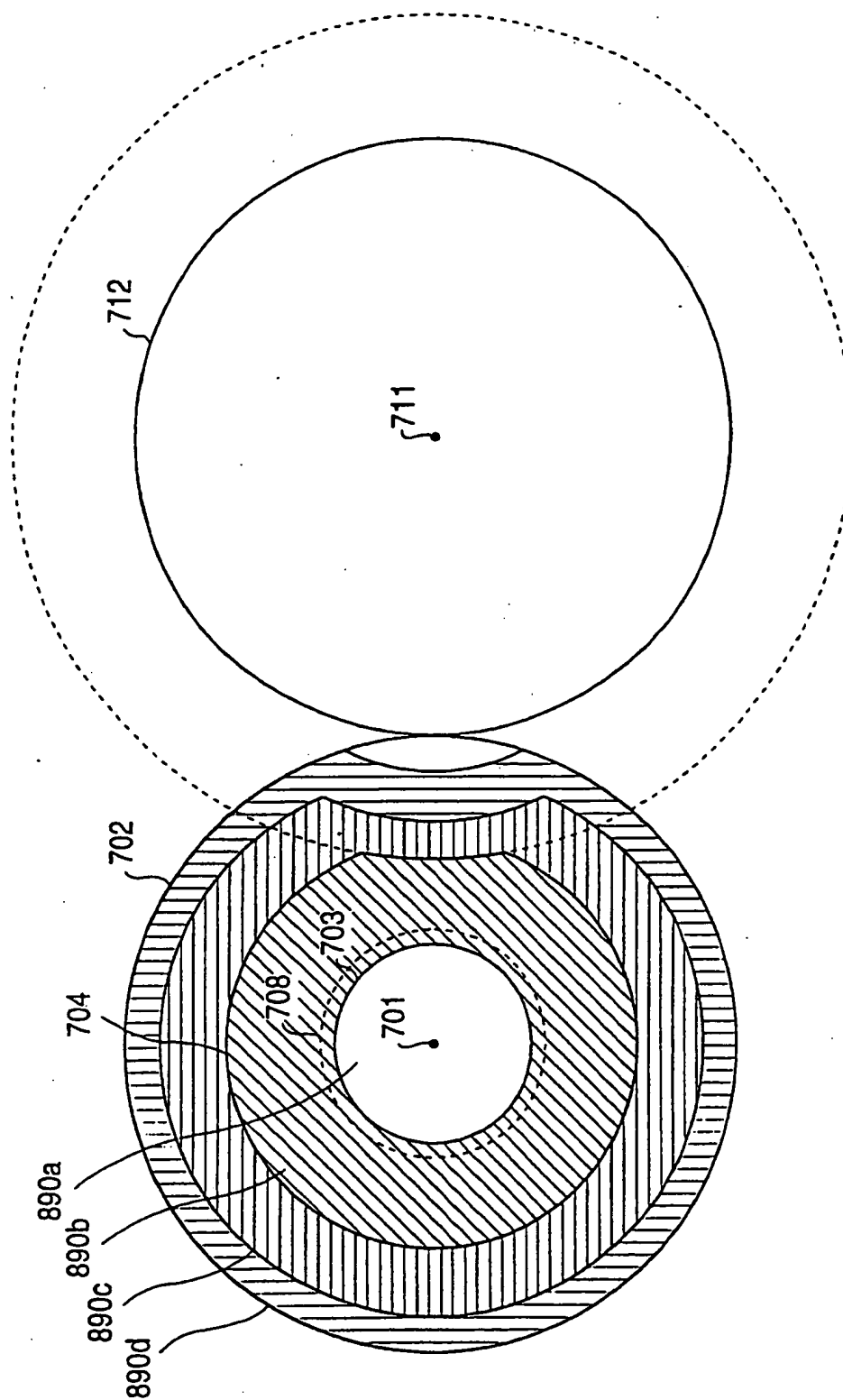


FIG. 91



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FIG. 92

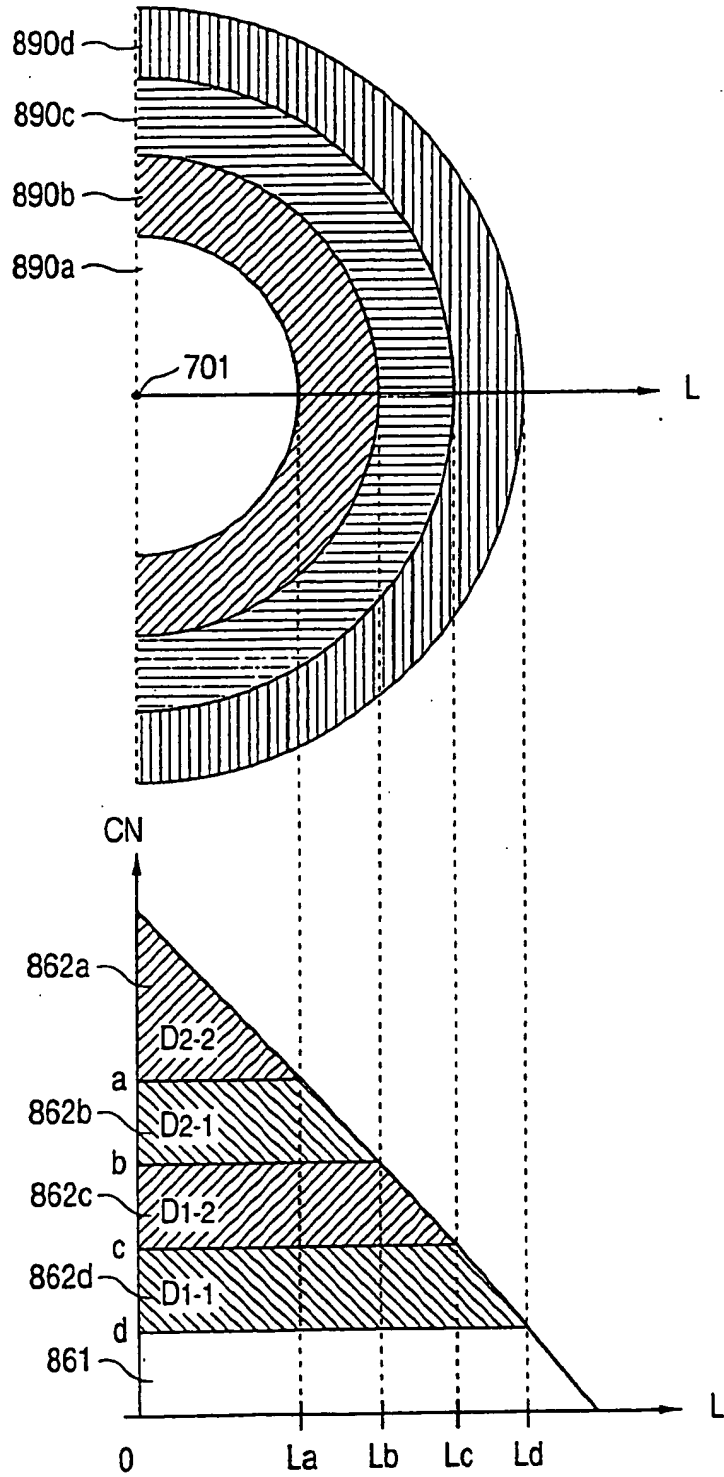


FIG. 93

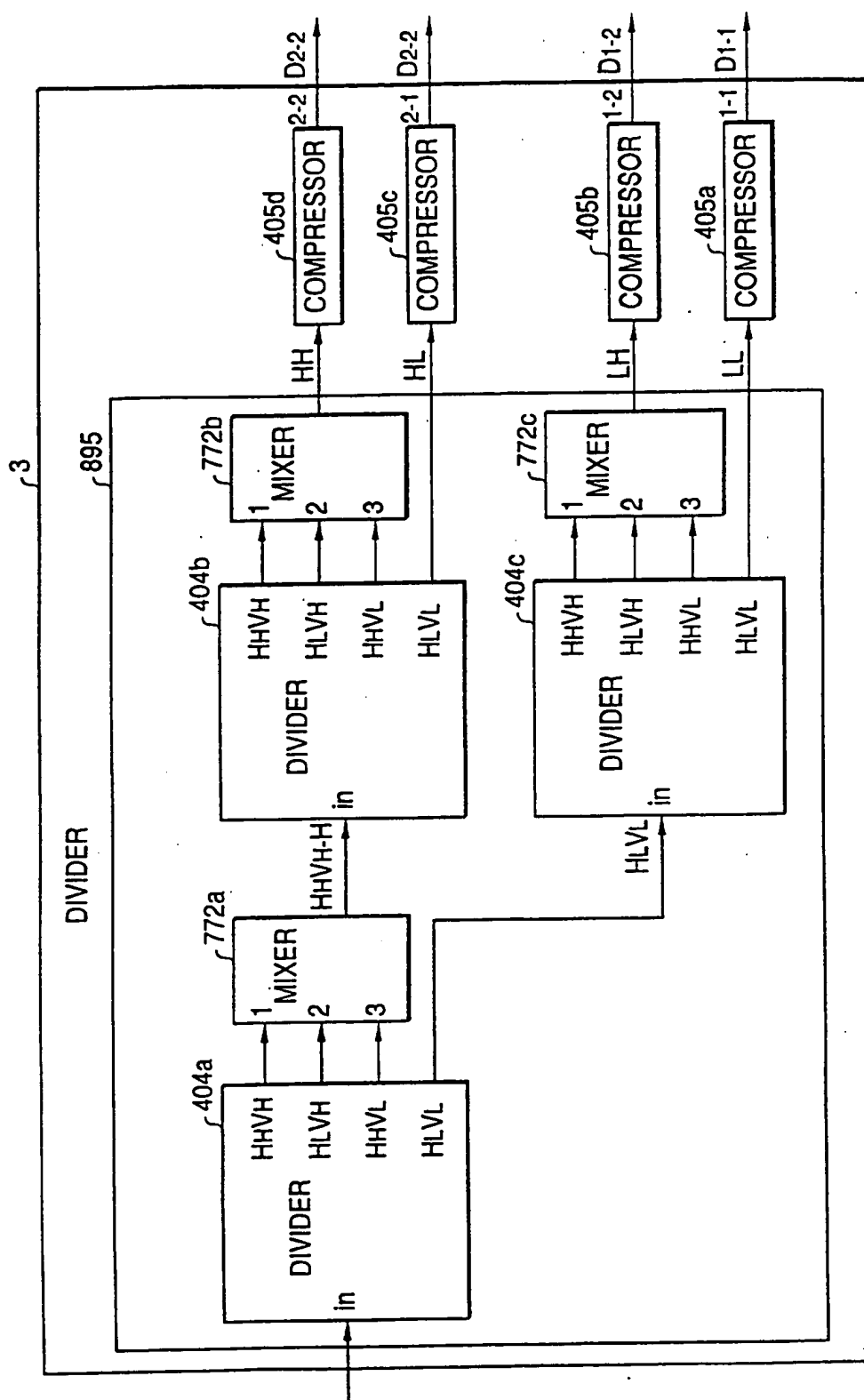


FIG. 94

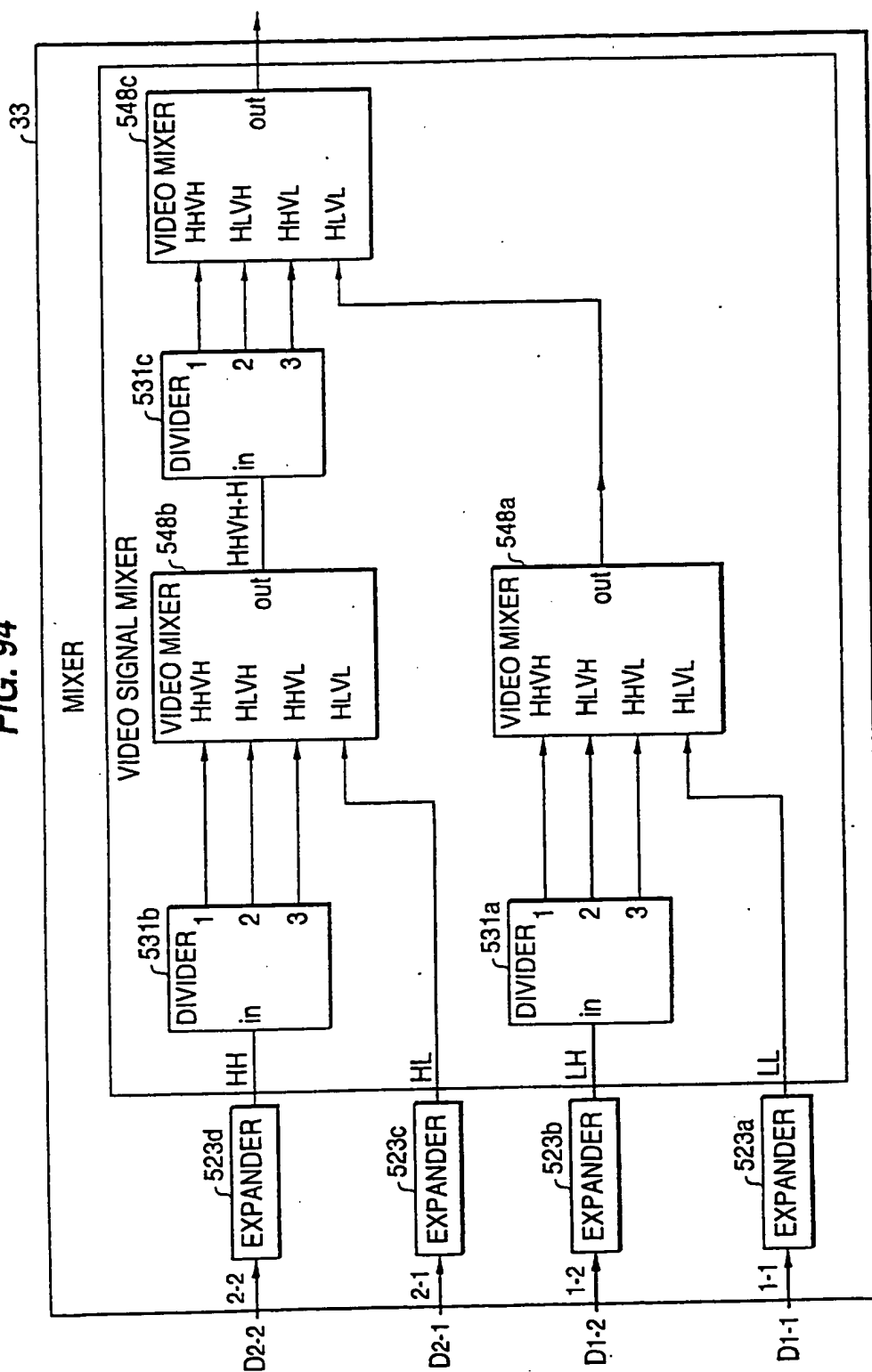


FIG. 95

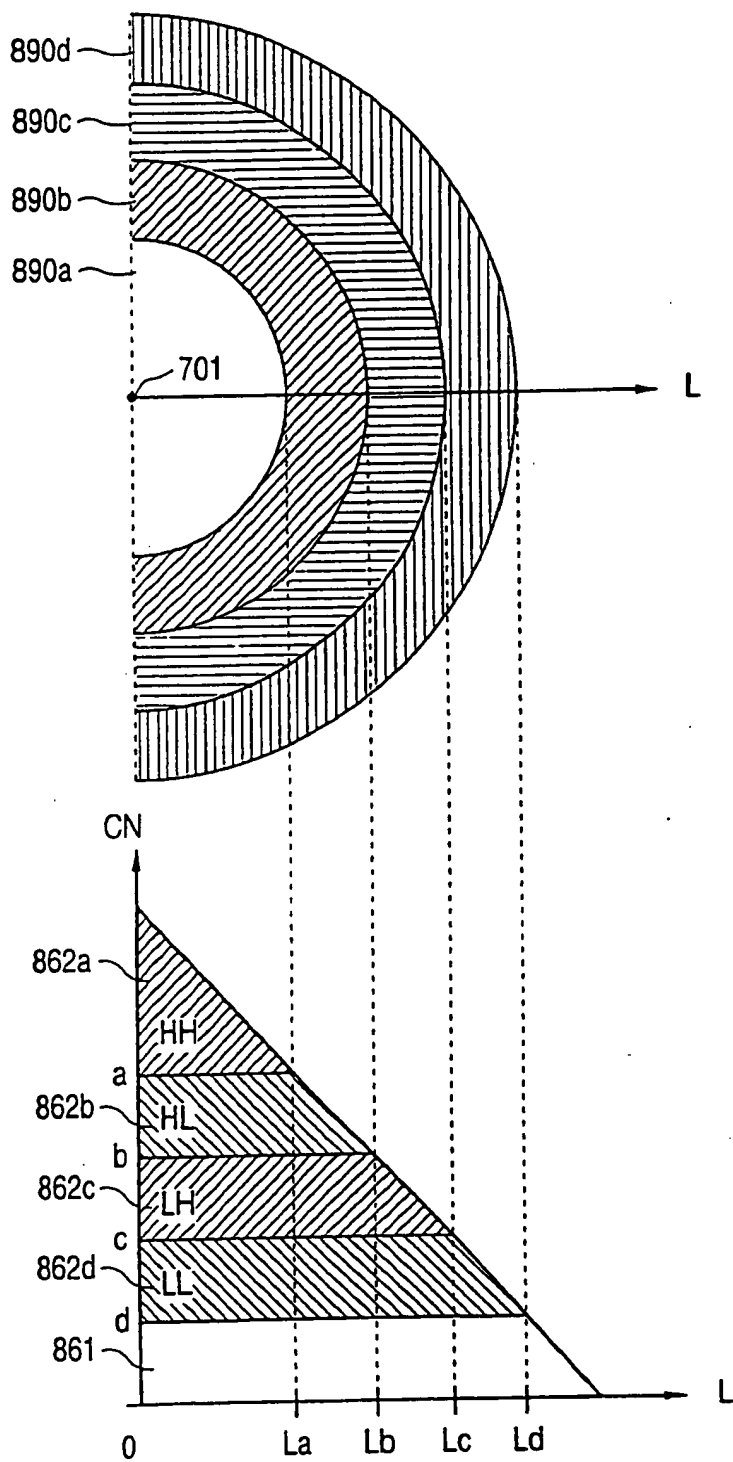


FIG. 96

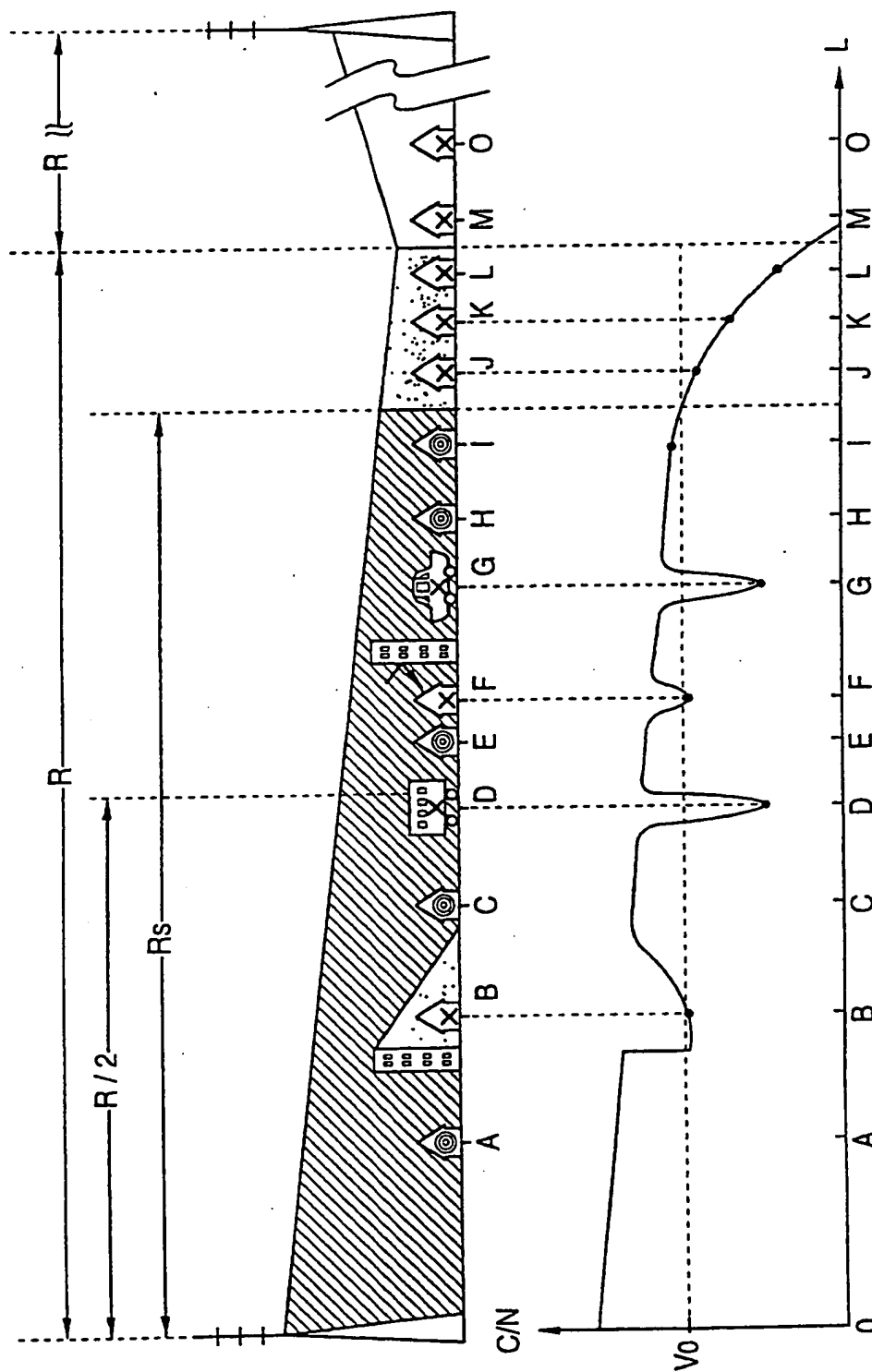


FIG. 97

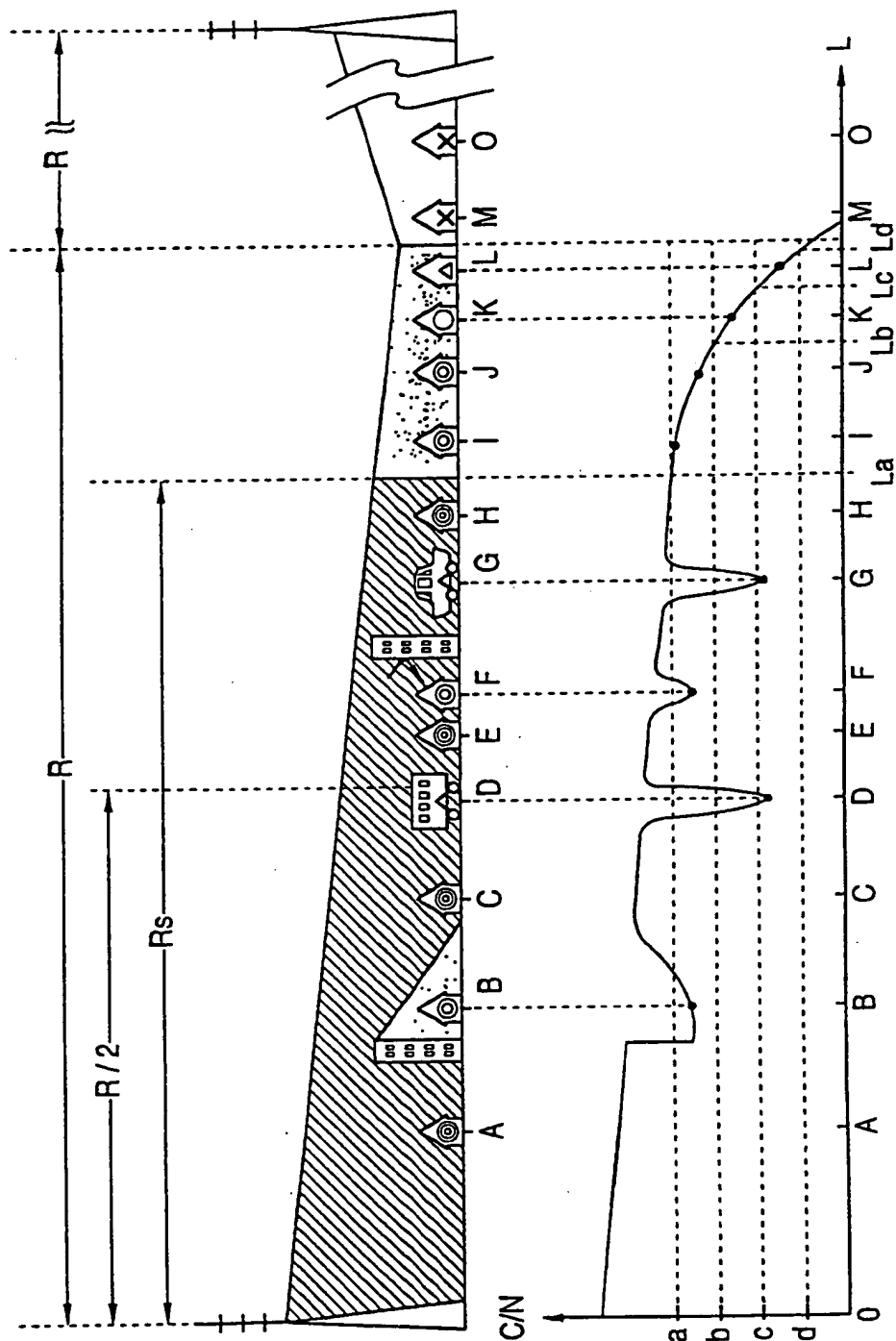


FIG. 98

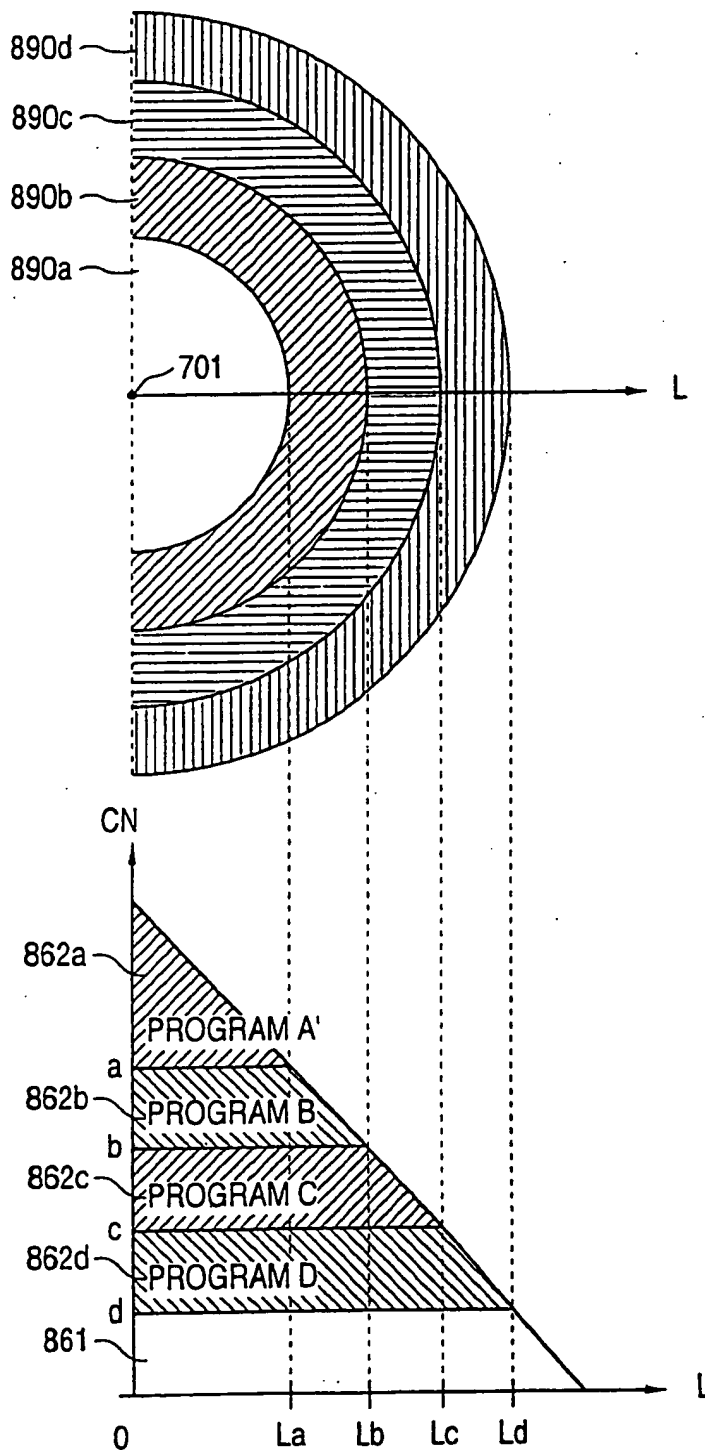


FIG. 99

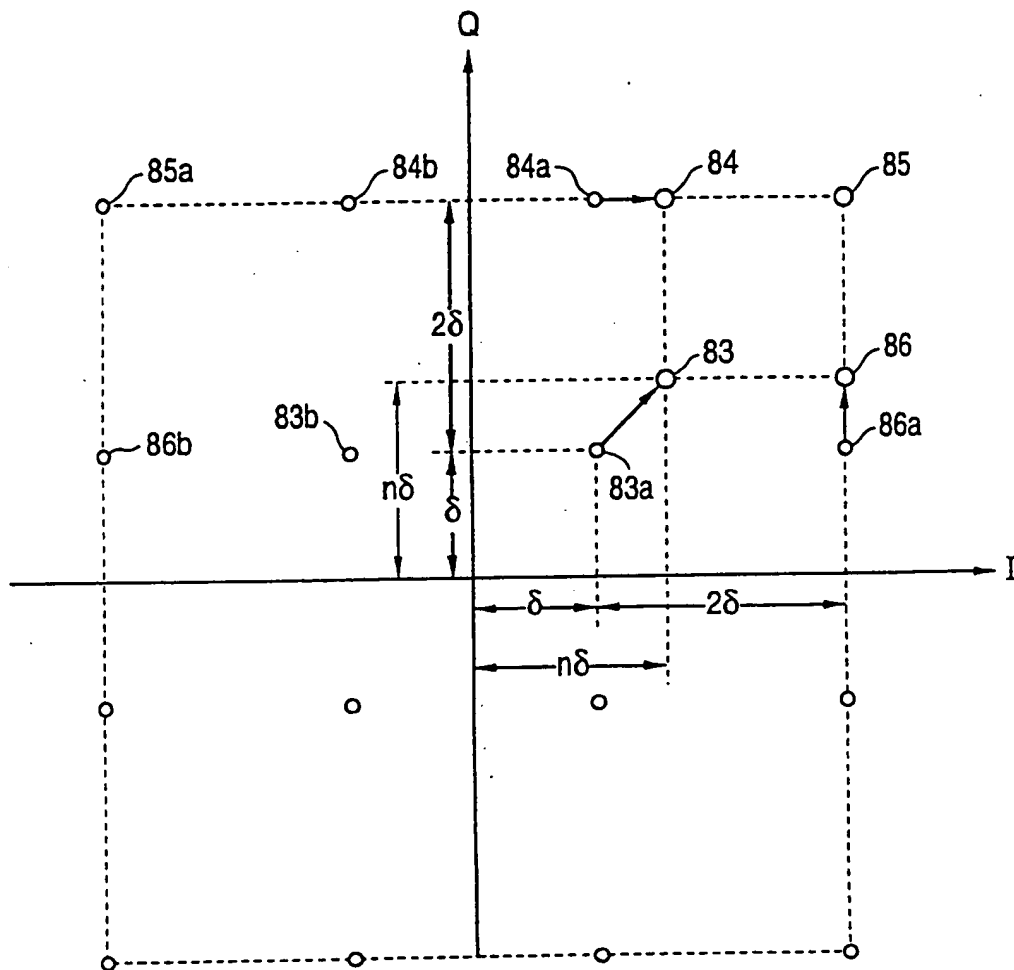


FIG. 100

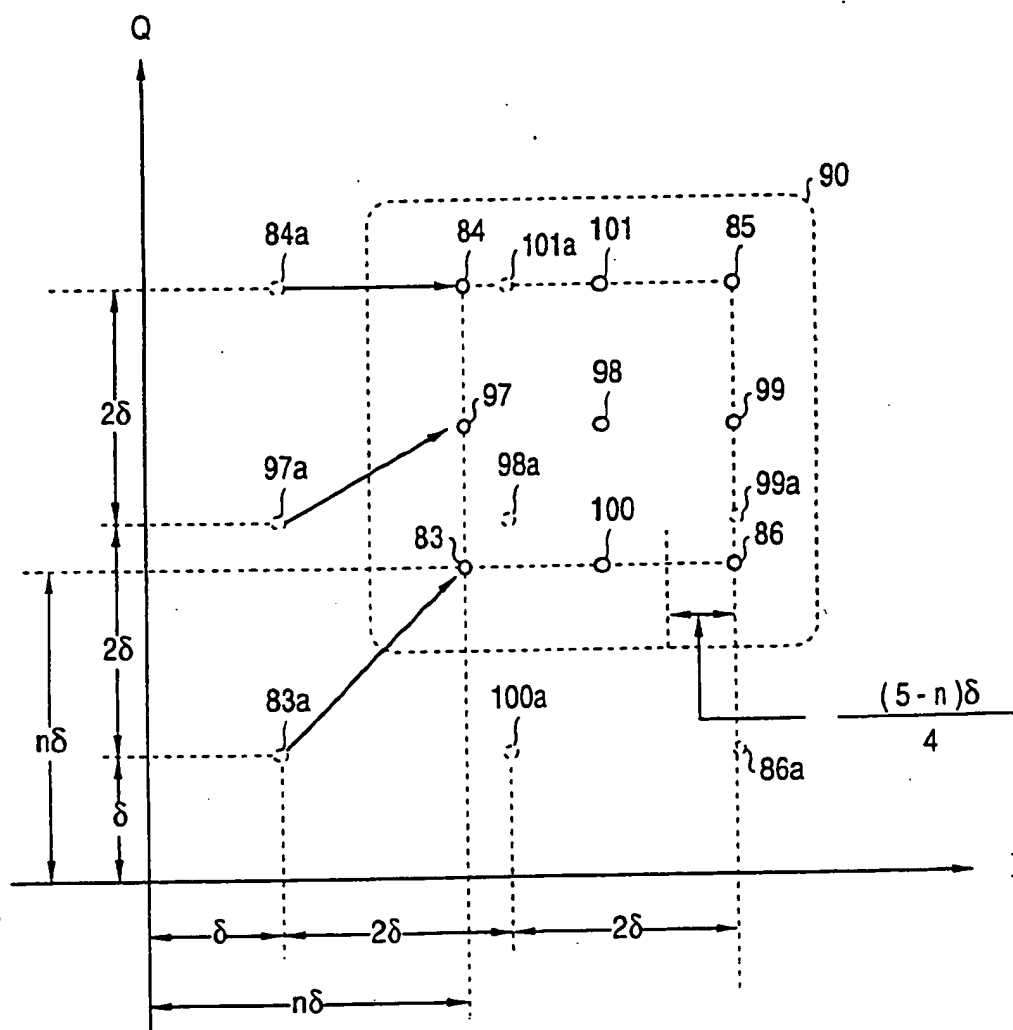


FIG. 101

Pe

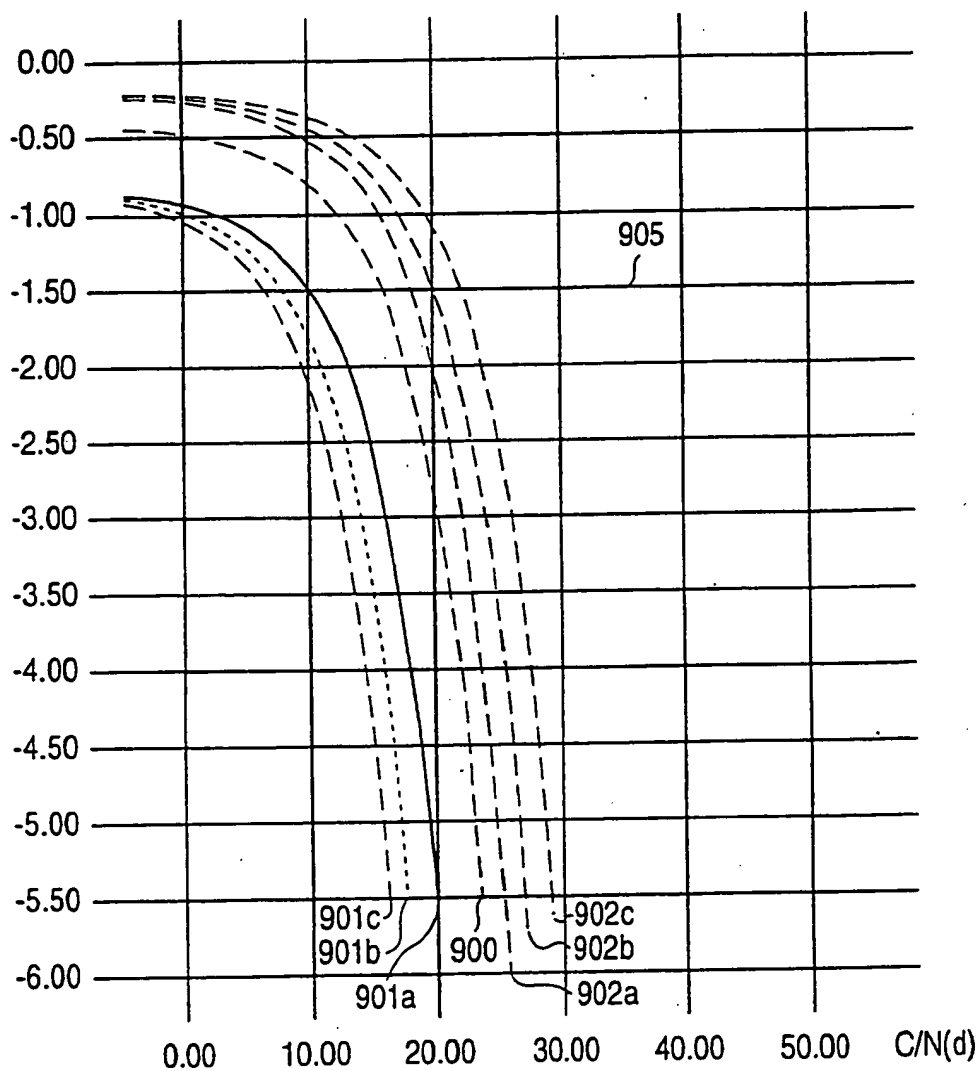


FIG. 102

Pe

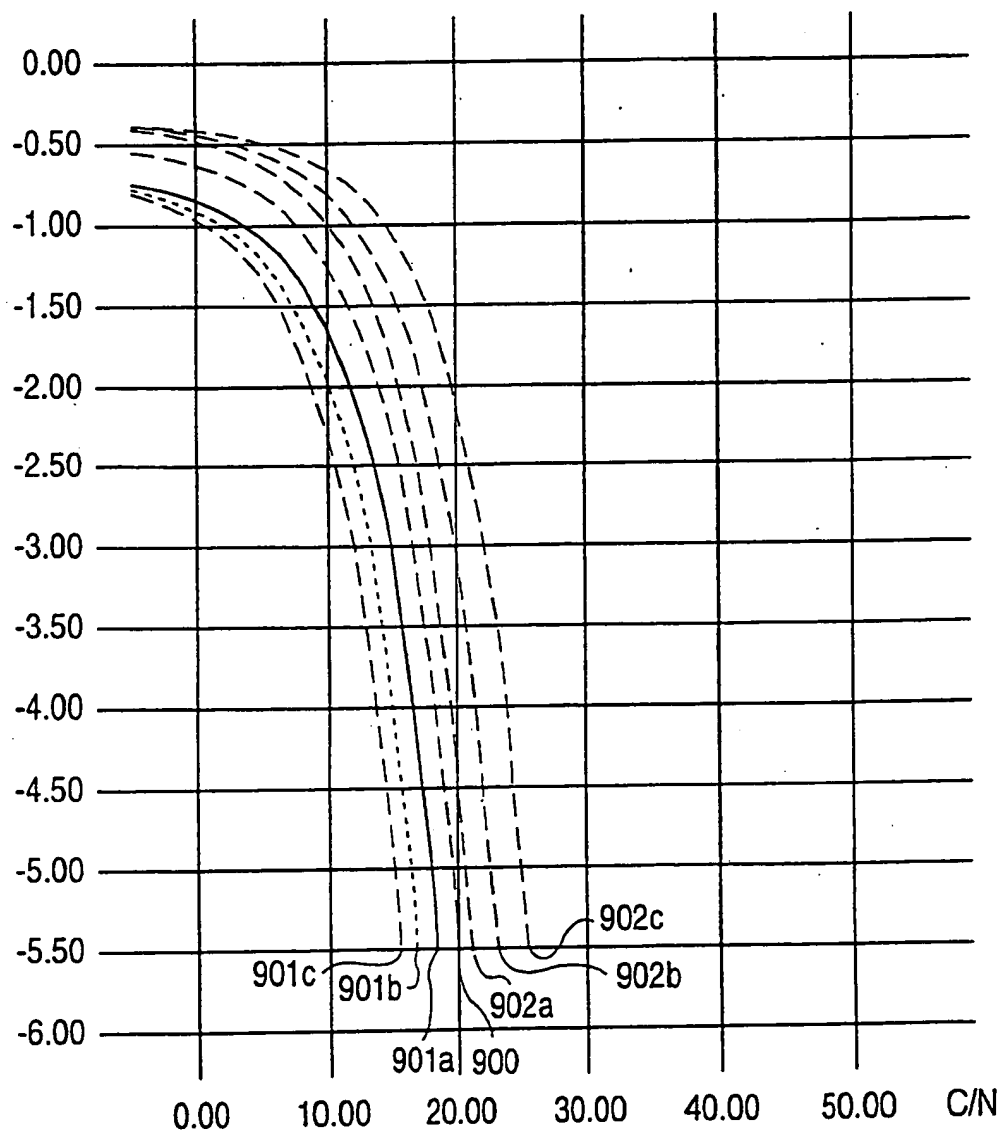


FIG. 103

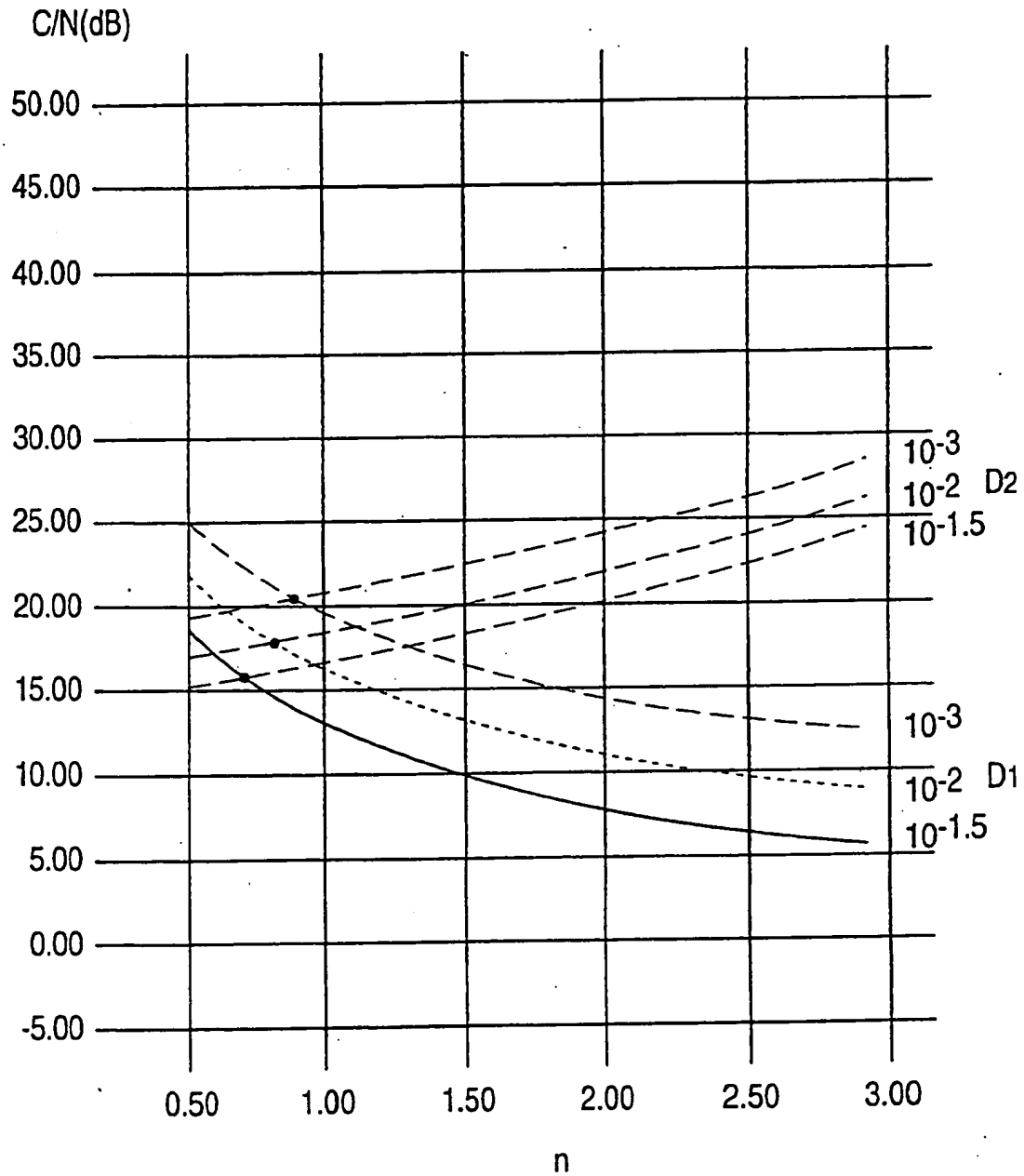


FIG. 104

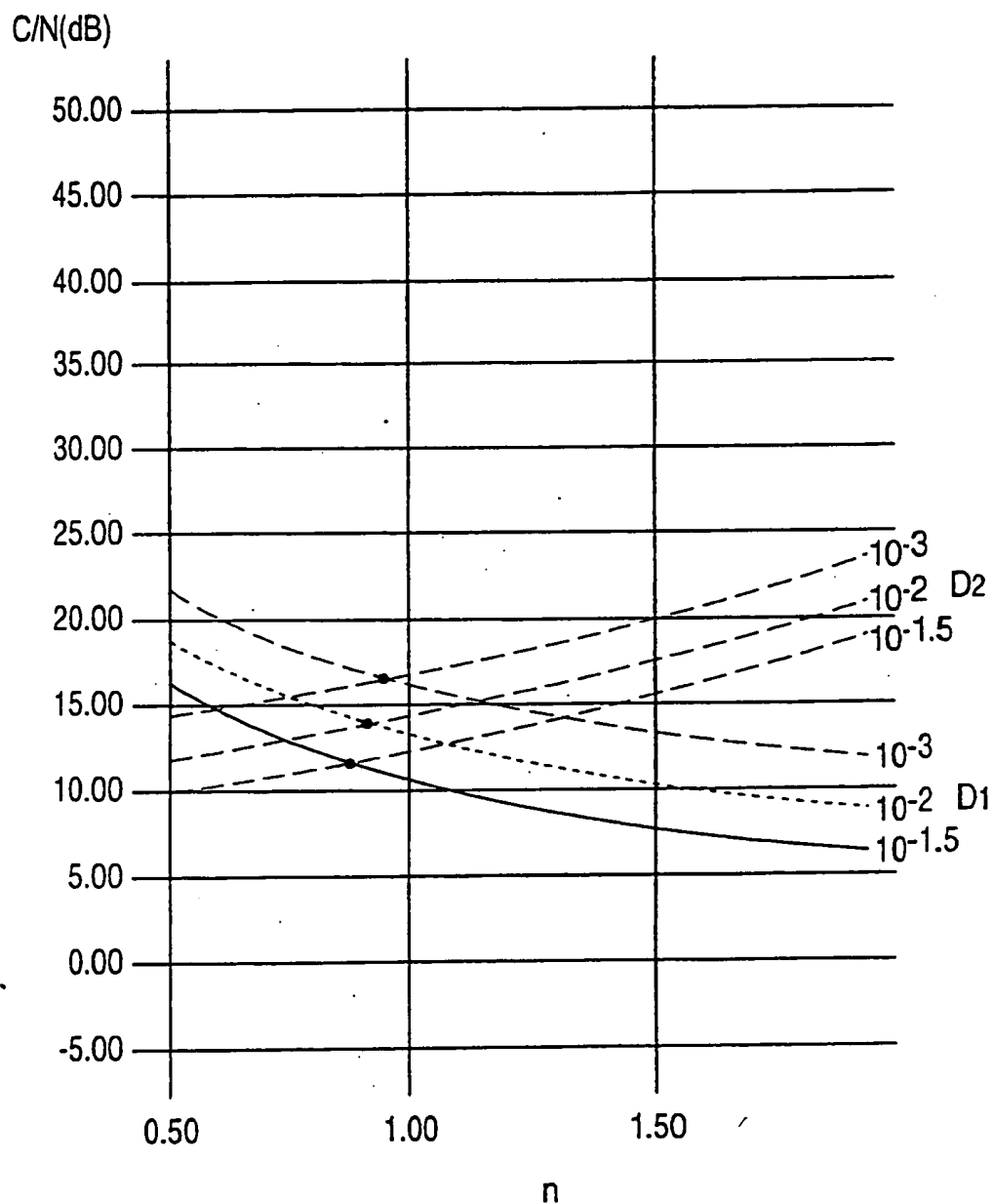


FIG. 105

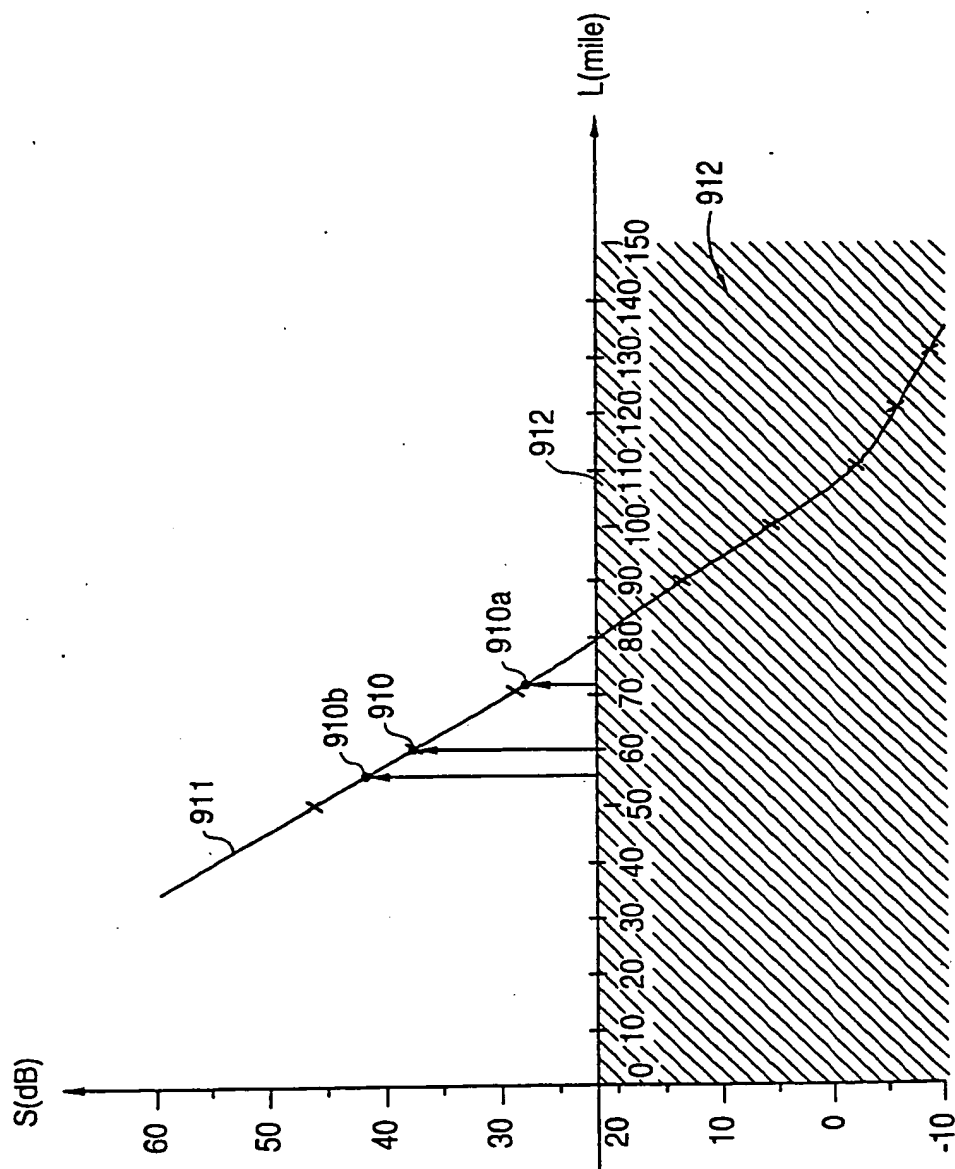


FIG. 106

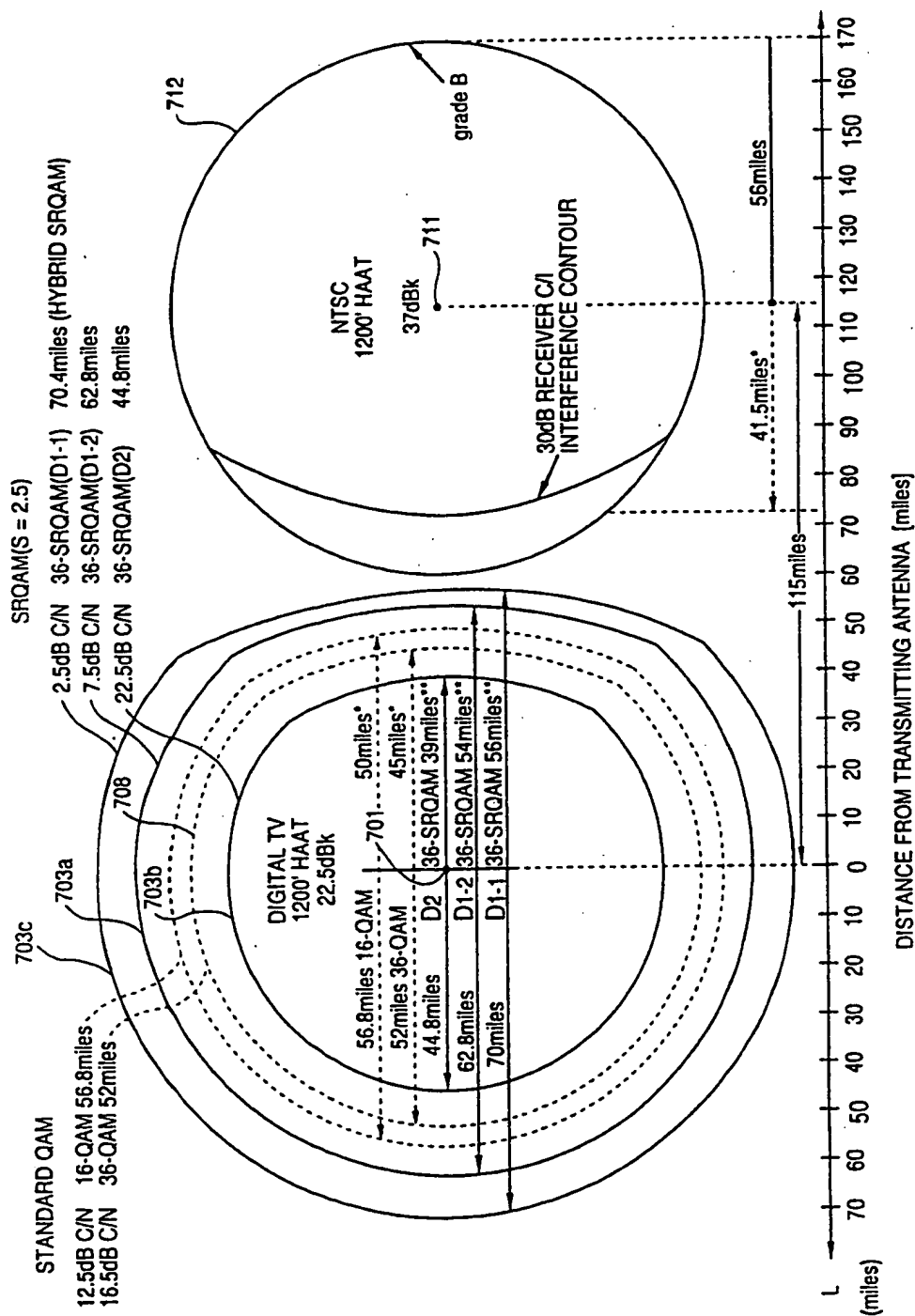


FIG. 107

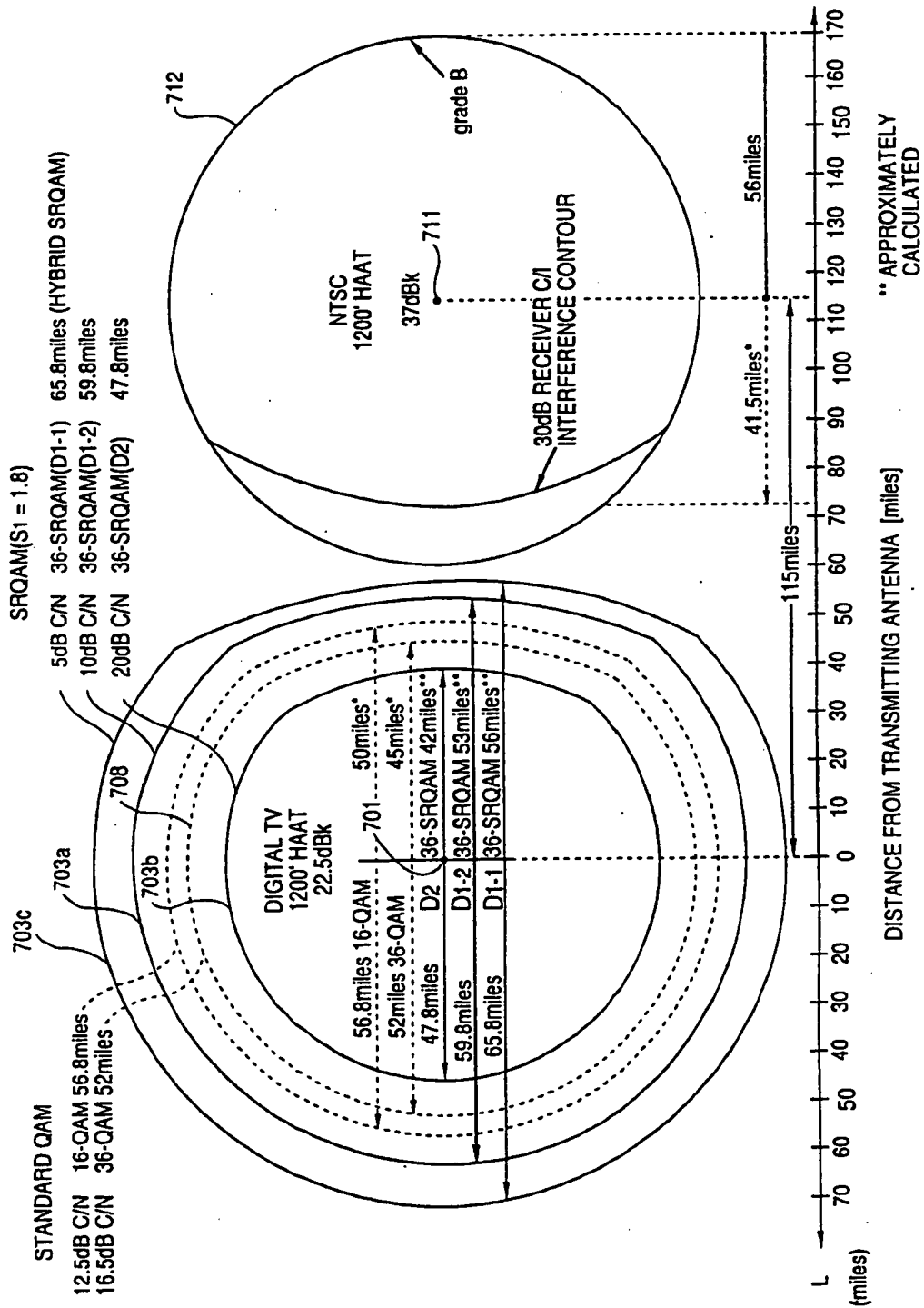


FIG. 108(a)

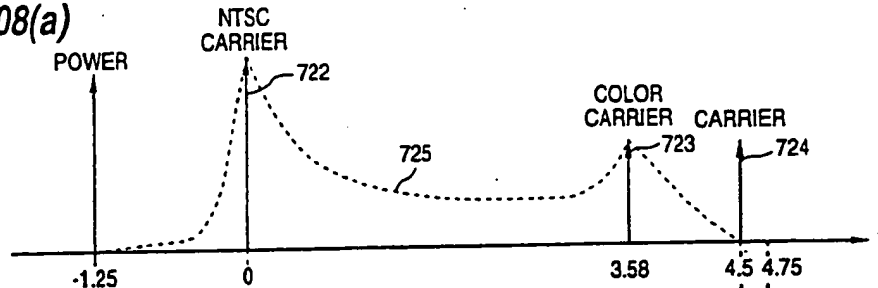


FIG. 108(b)

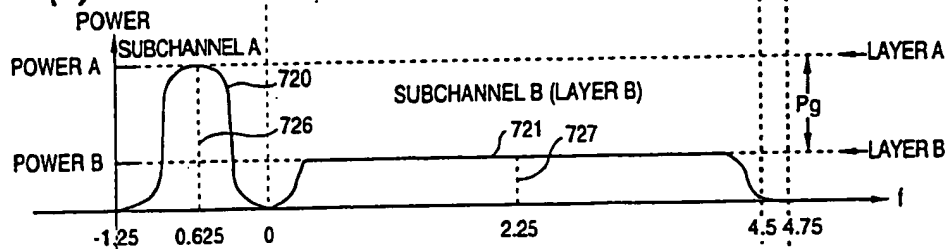


FIG. 108(c)

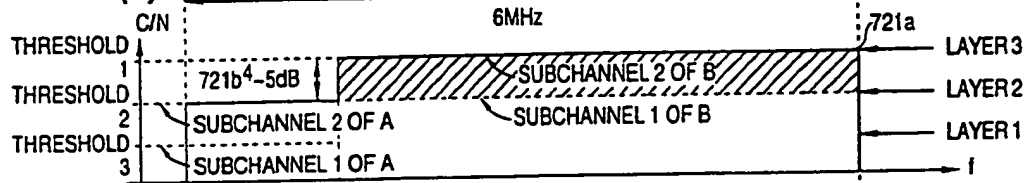


FIG. 108(d)

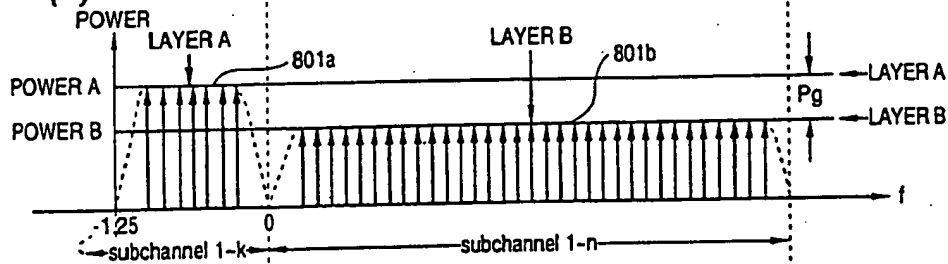


FIG. 108(e)

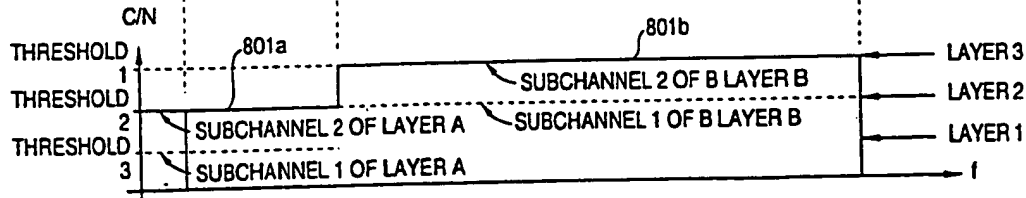
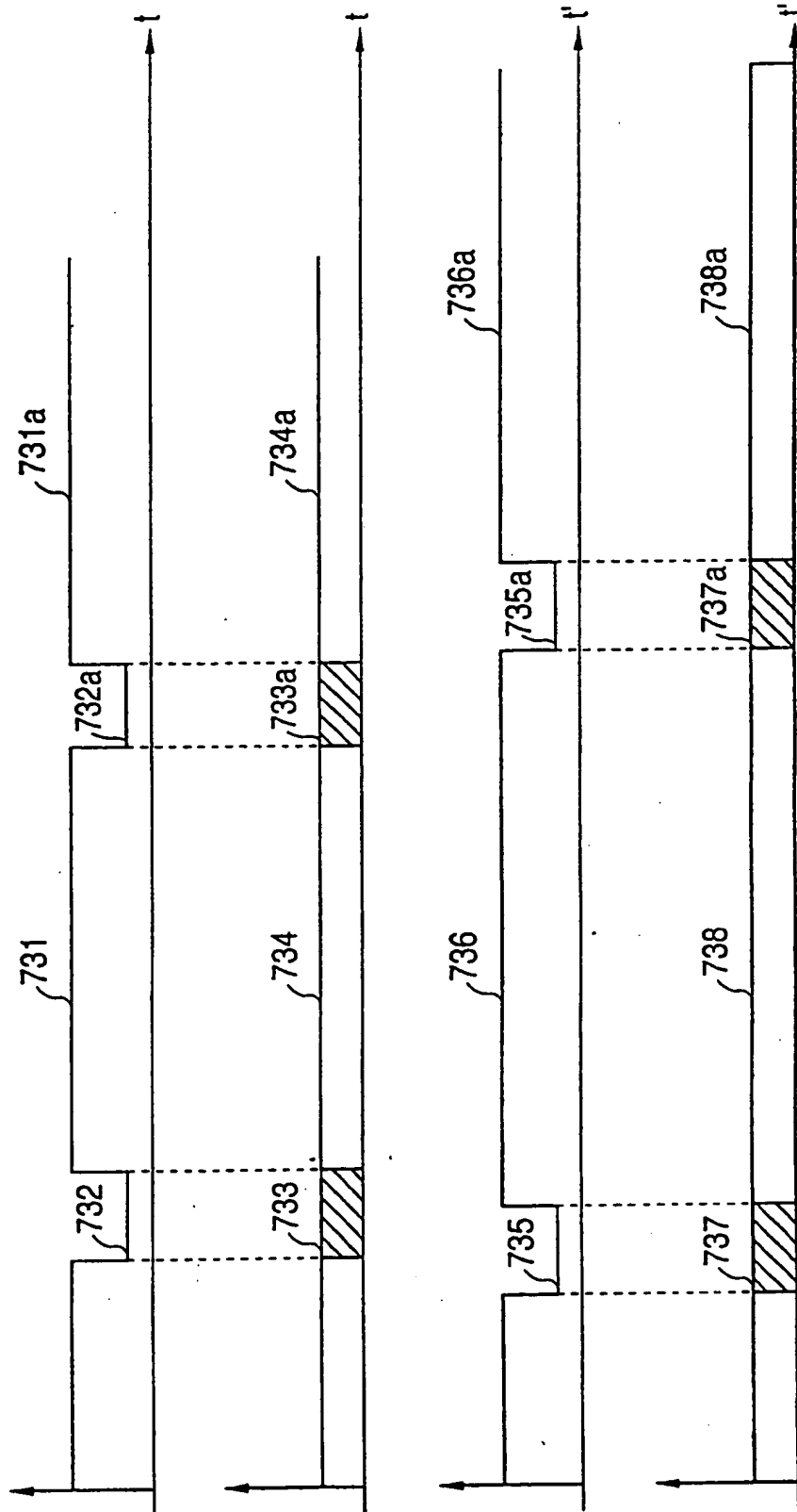


FIG. 109



[illegible]

FIG. 110

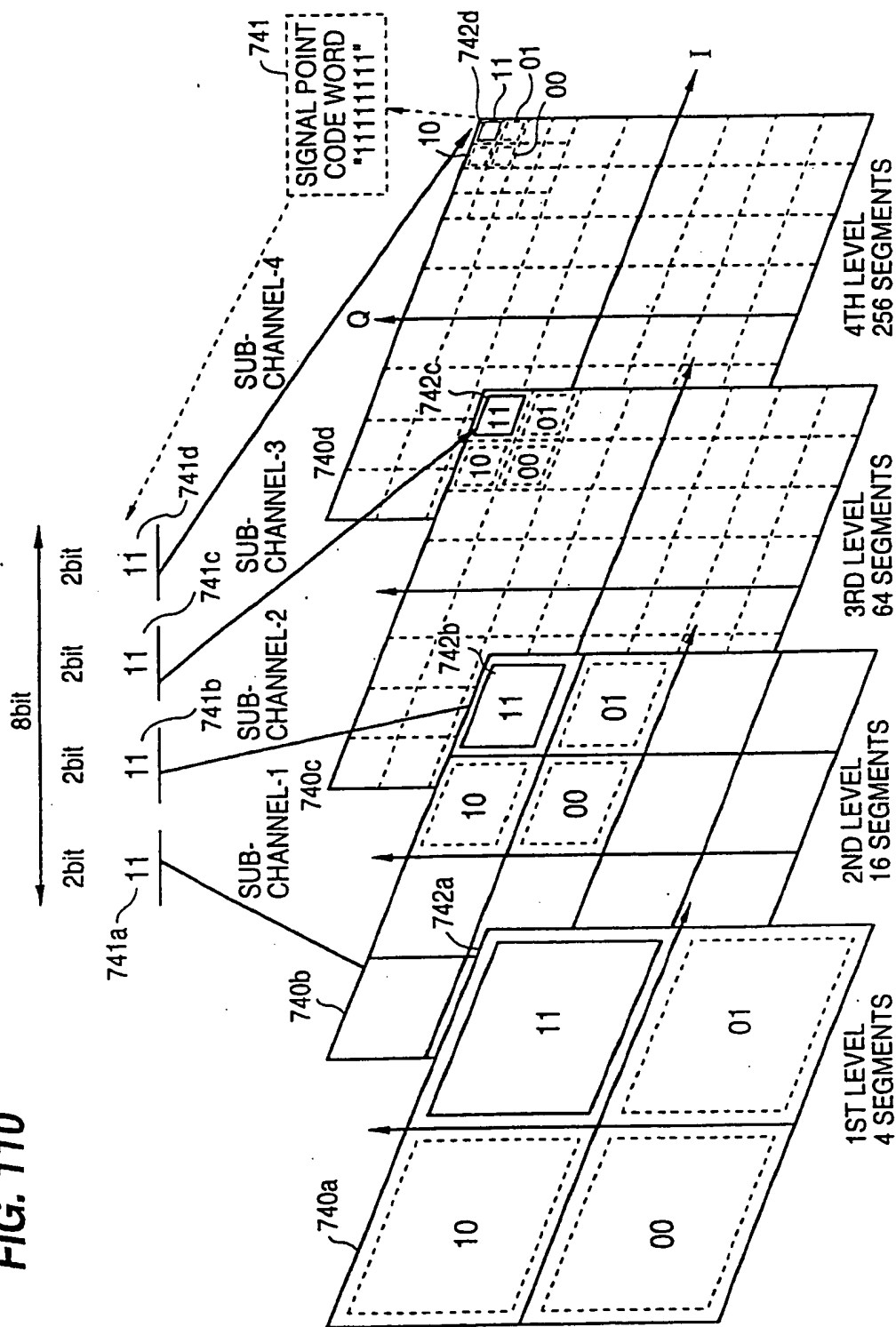
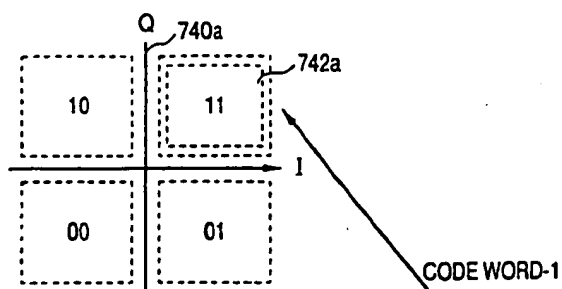
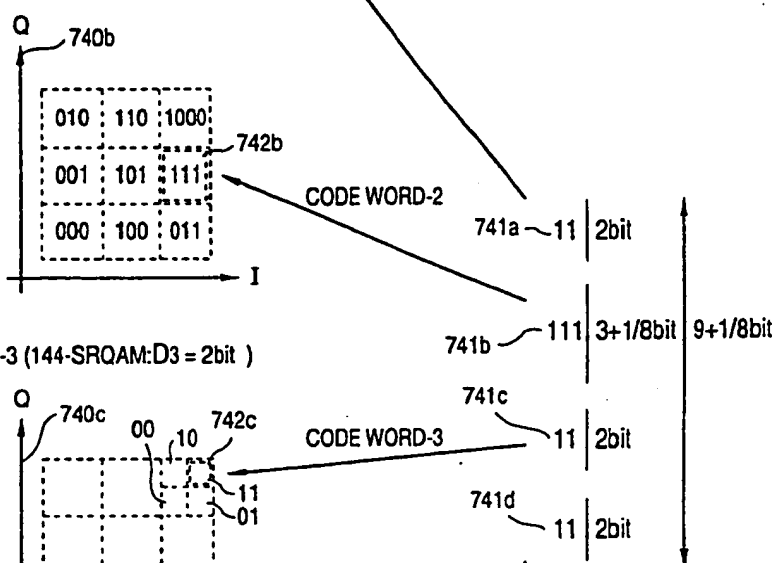


FIG. 111

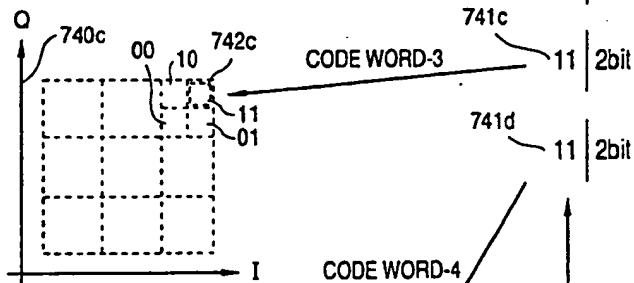
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



SUBCHANNEL-2 (36-SRQAM:D2 = 3bit + 1/8bit)



SUBCHANNEL-3 (144-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (576-SRQAM:D4 = 2bit)

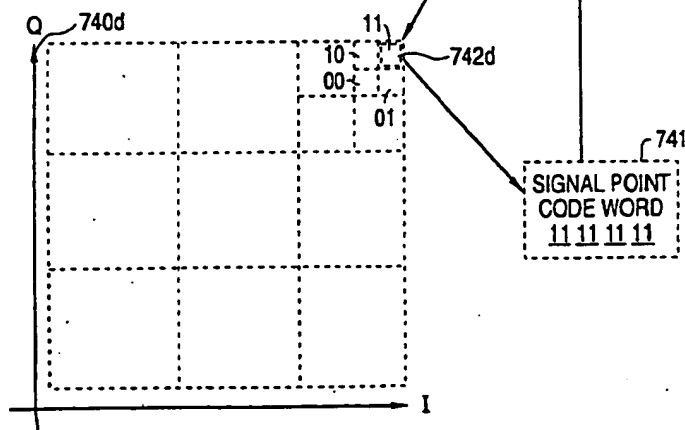
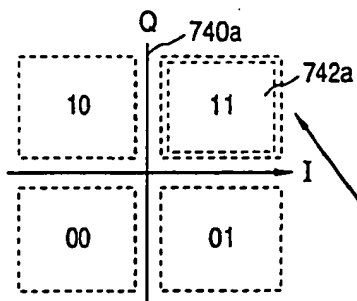
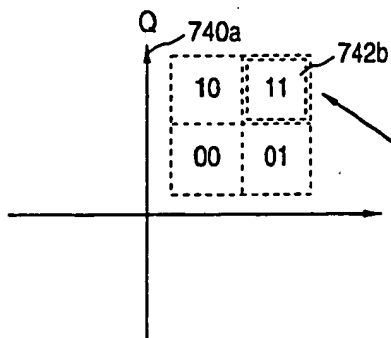


FIG. 112

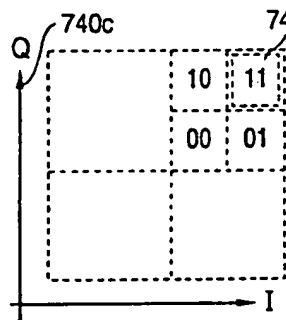
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



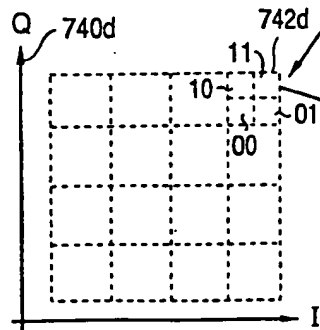
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)

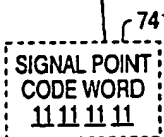
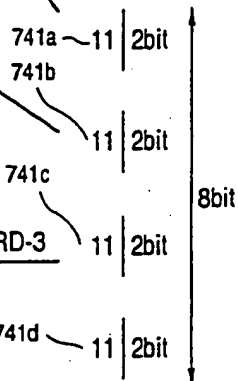


CODE WORD-1

CODE WORD-2

CODE WORD-3

CODE WORD-4



000001 100000

FIG. 113

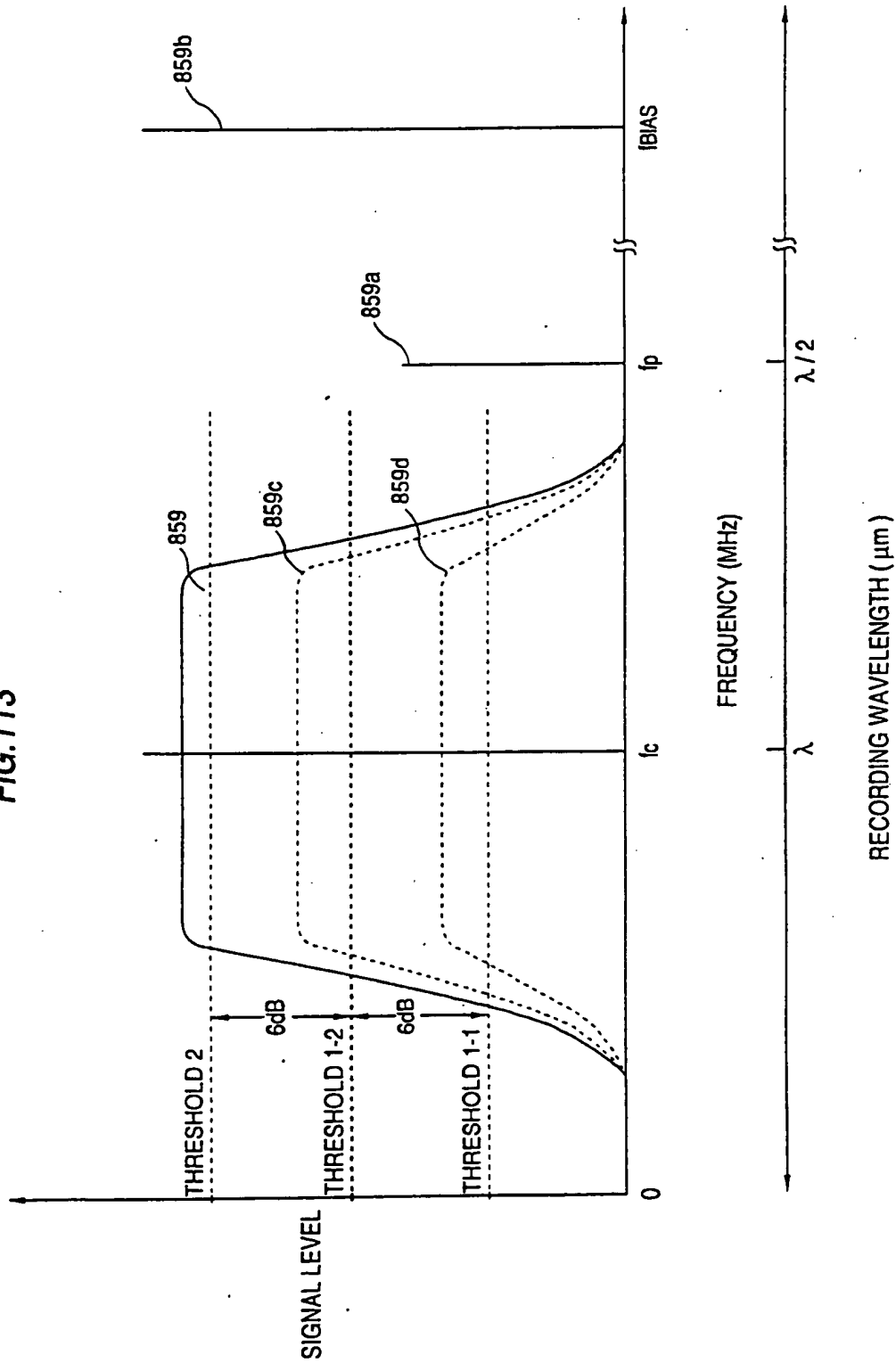


FIG. 114

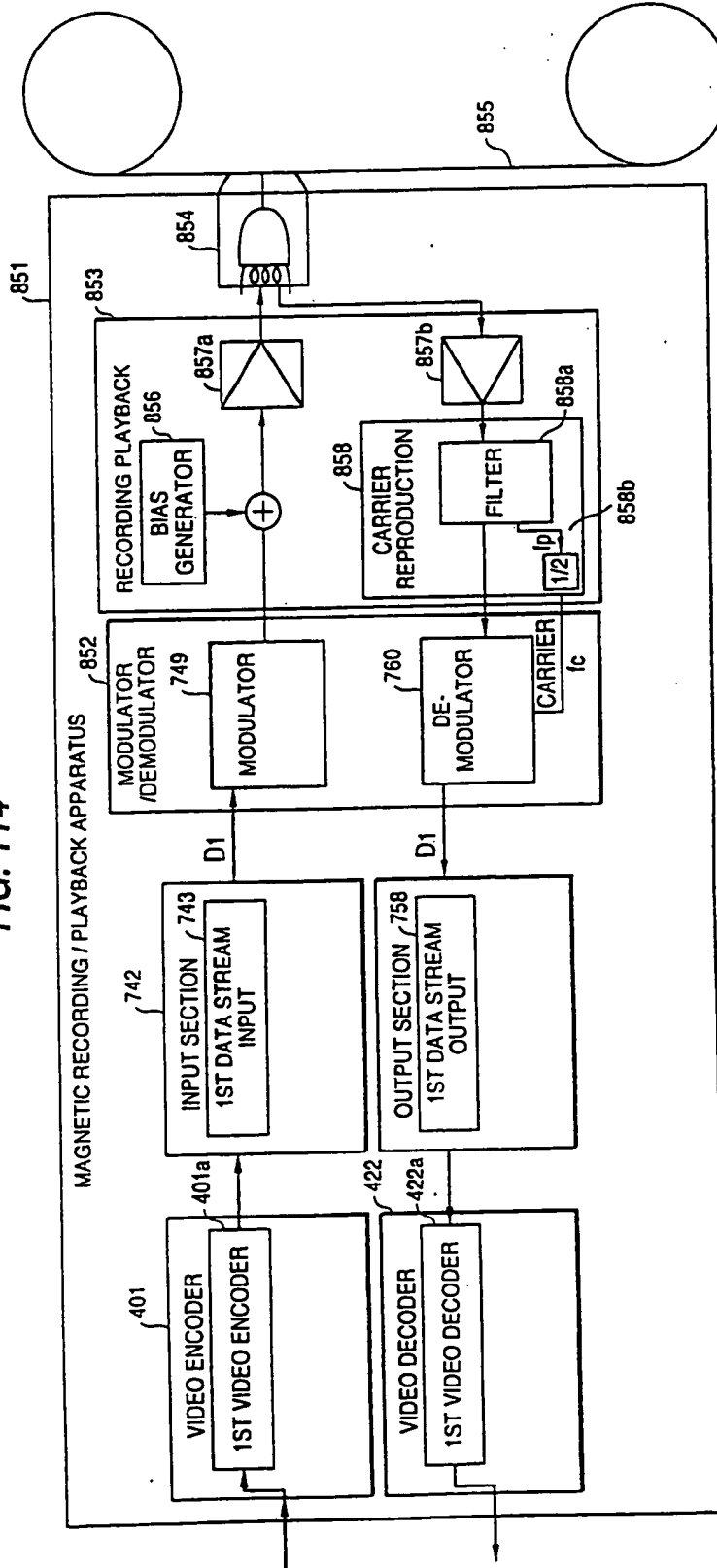


FIG. 115

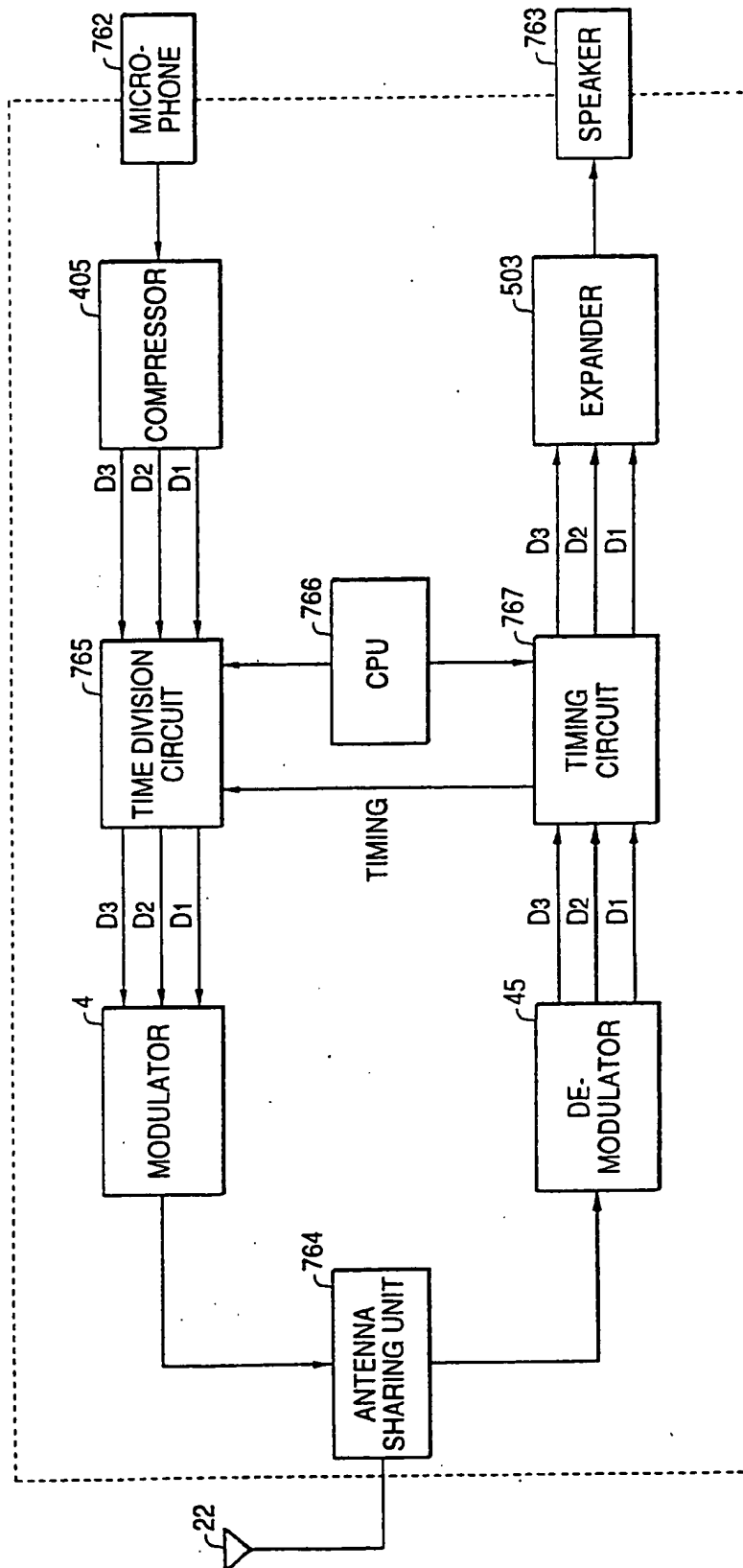


FIG. 116

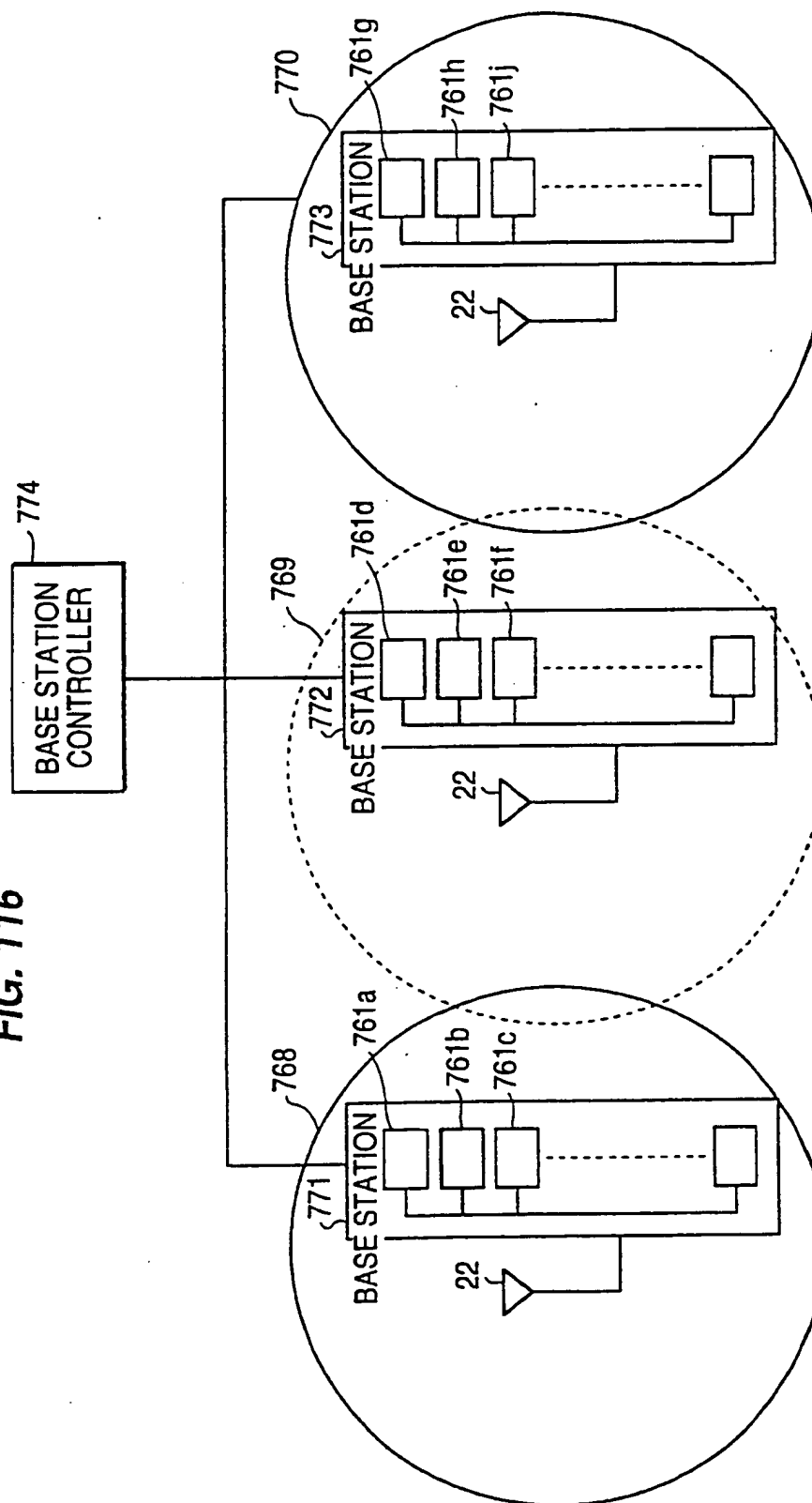
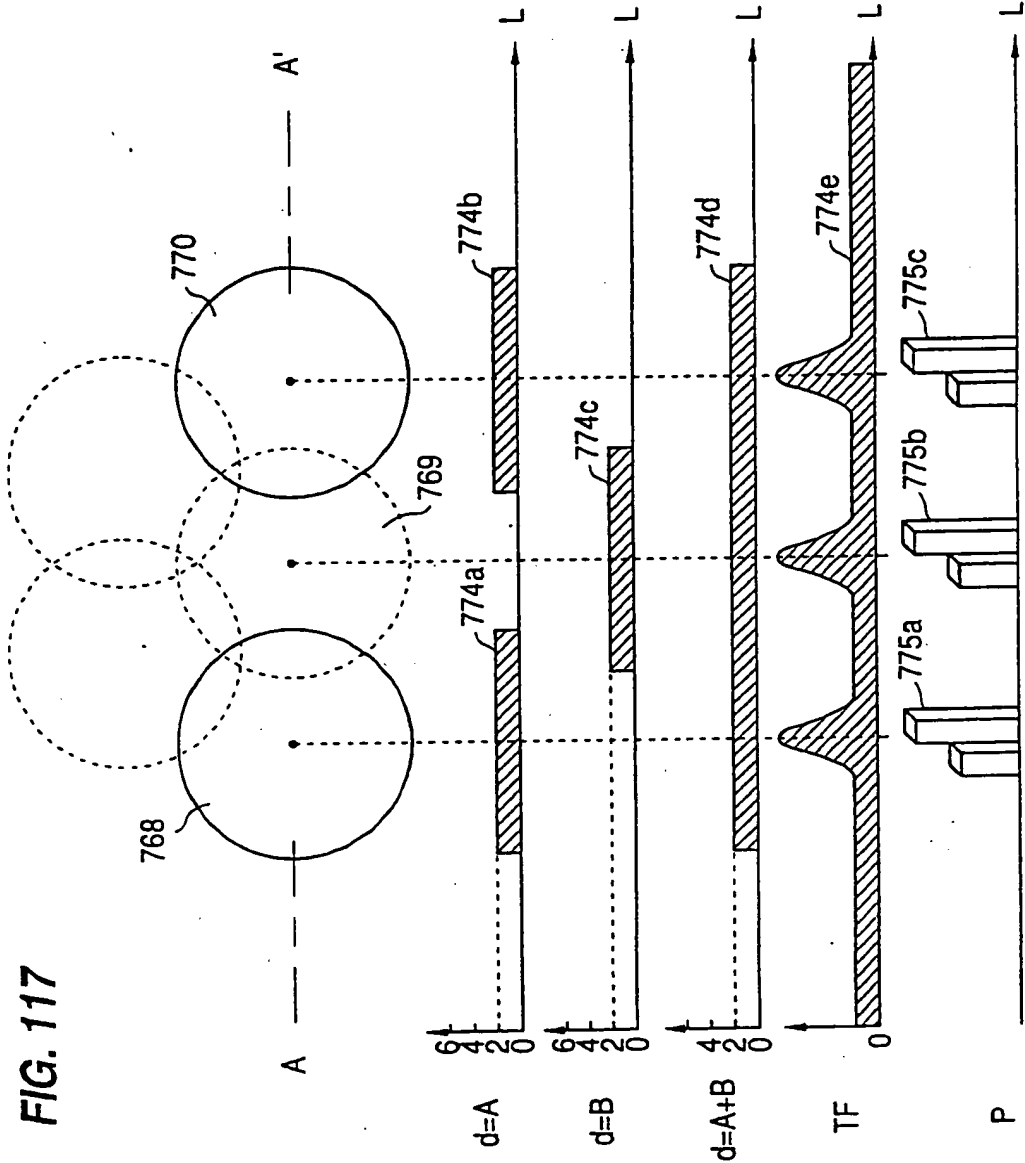


FIG. 117



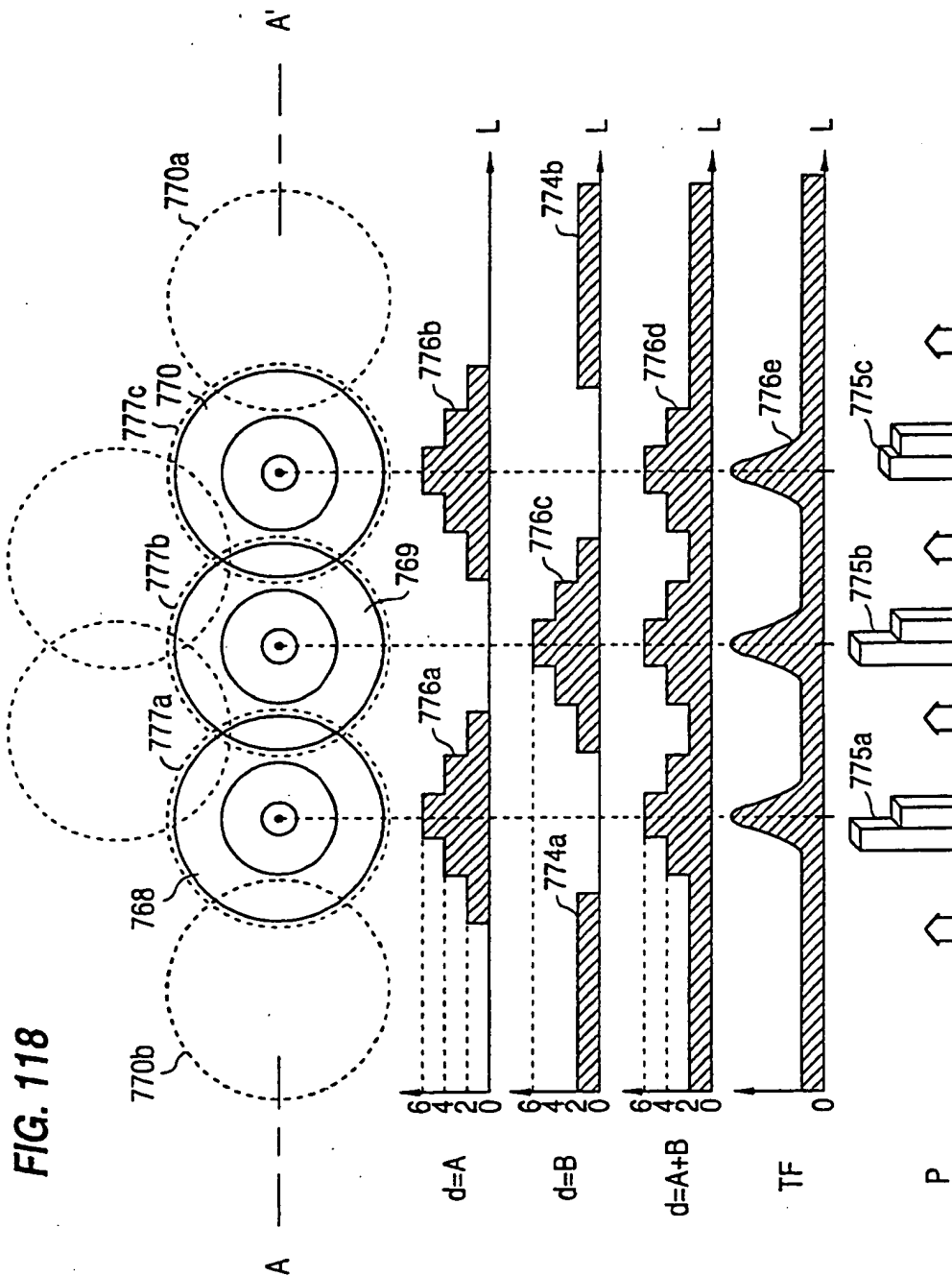


FIG. 119(a)

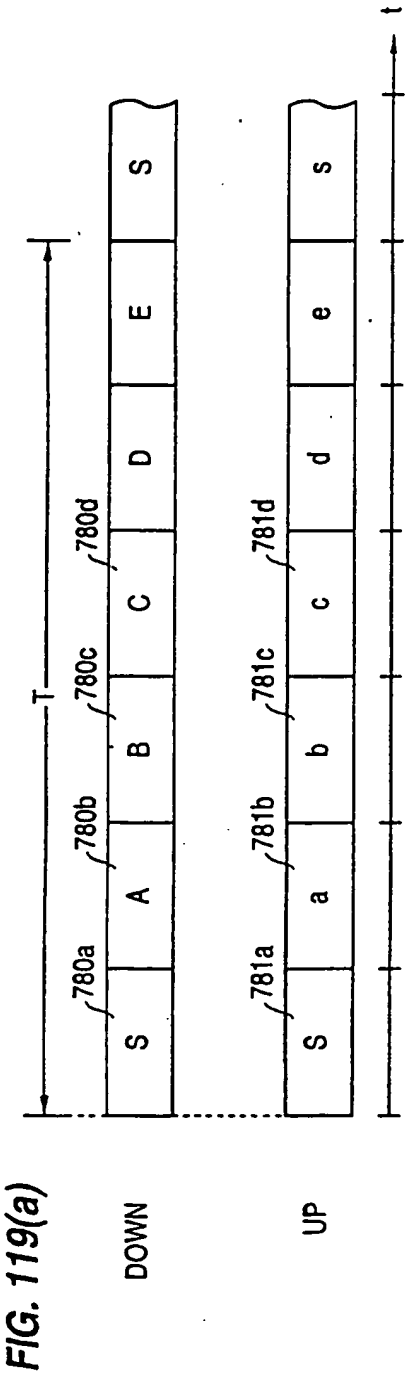
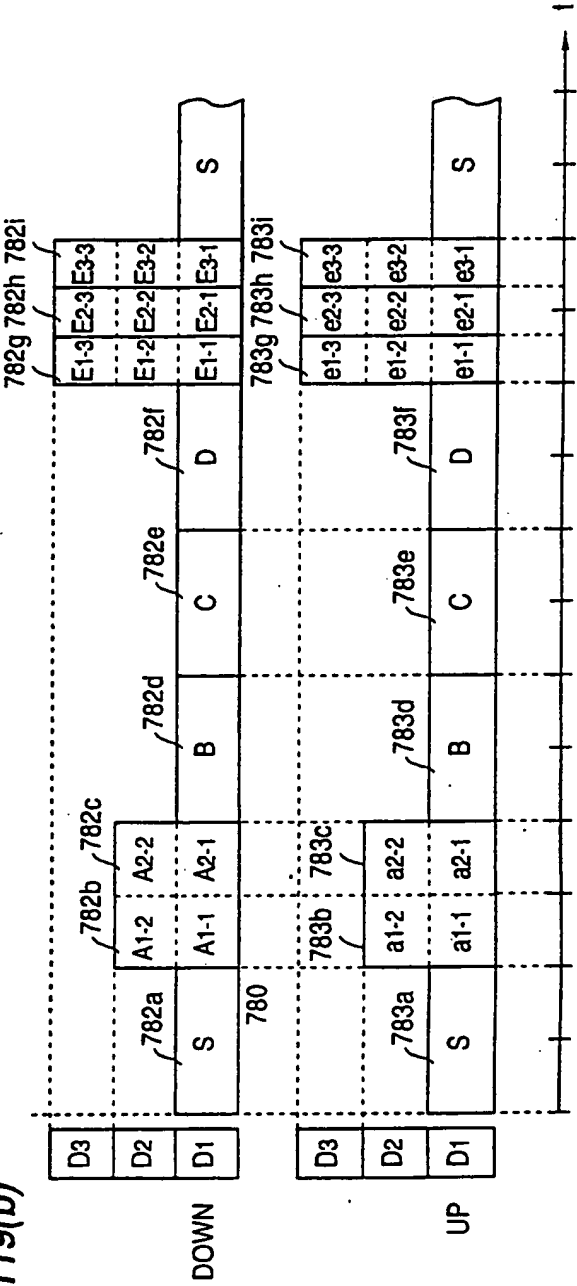


FIG. 119(b)



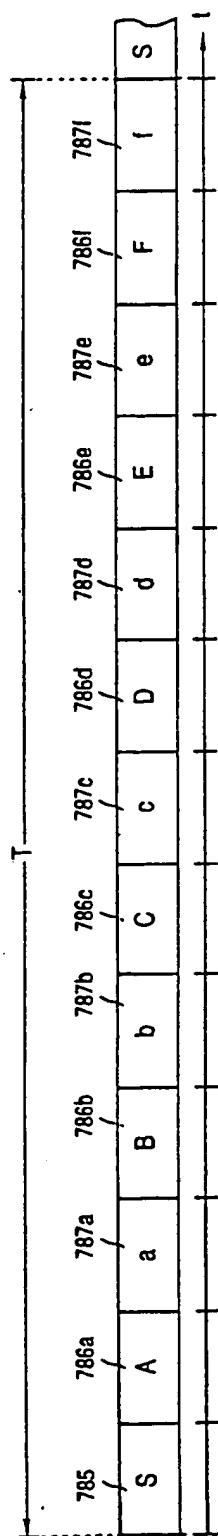


FIG. 120(b)

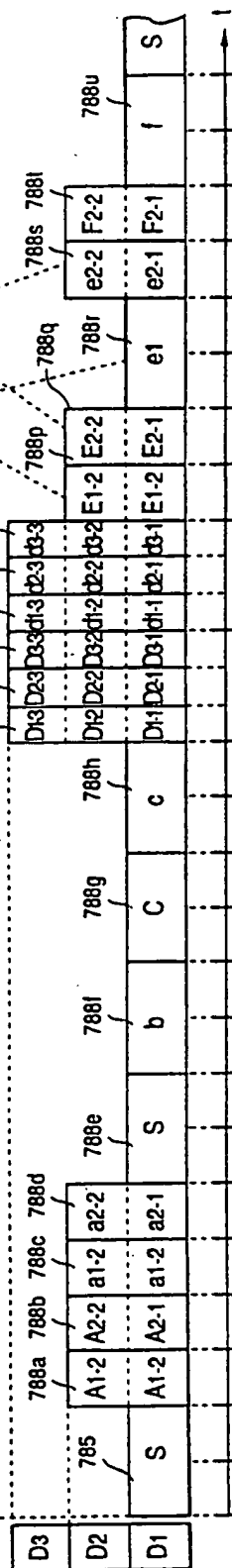


FIG. 121

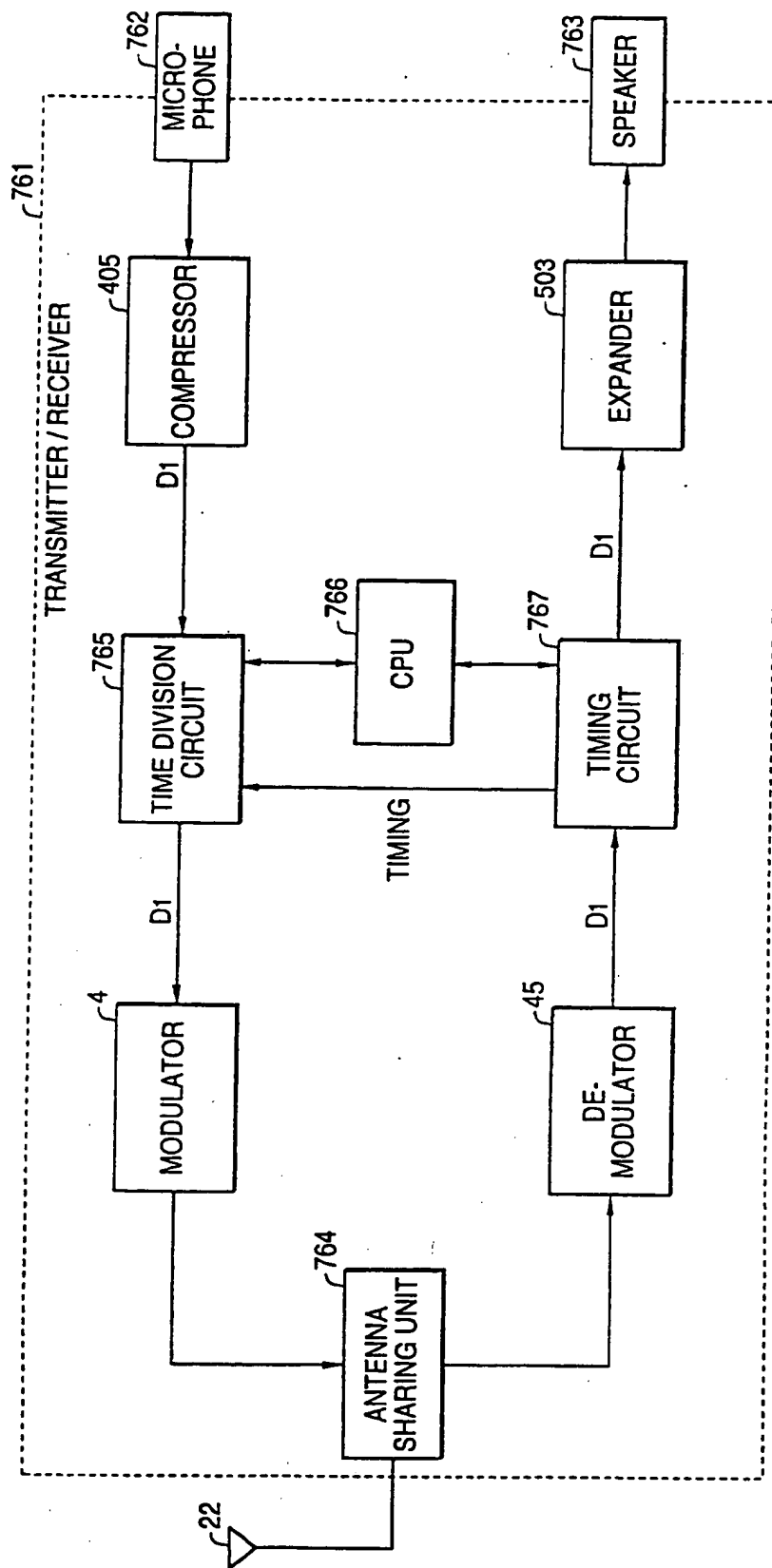
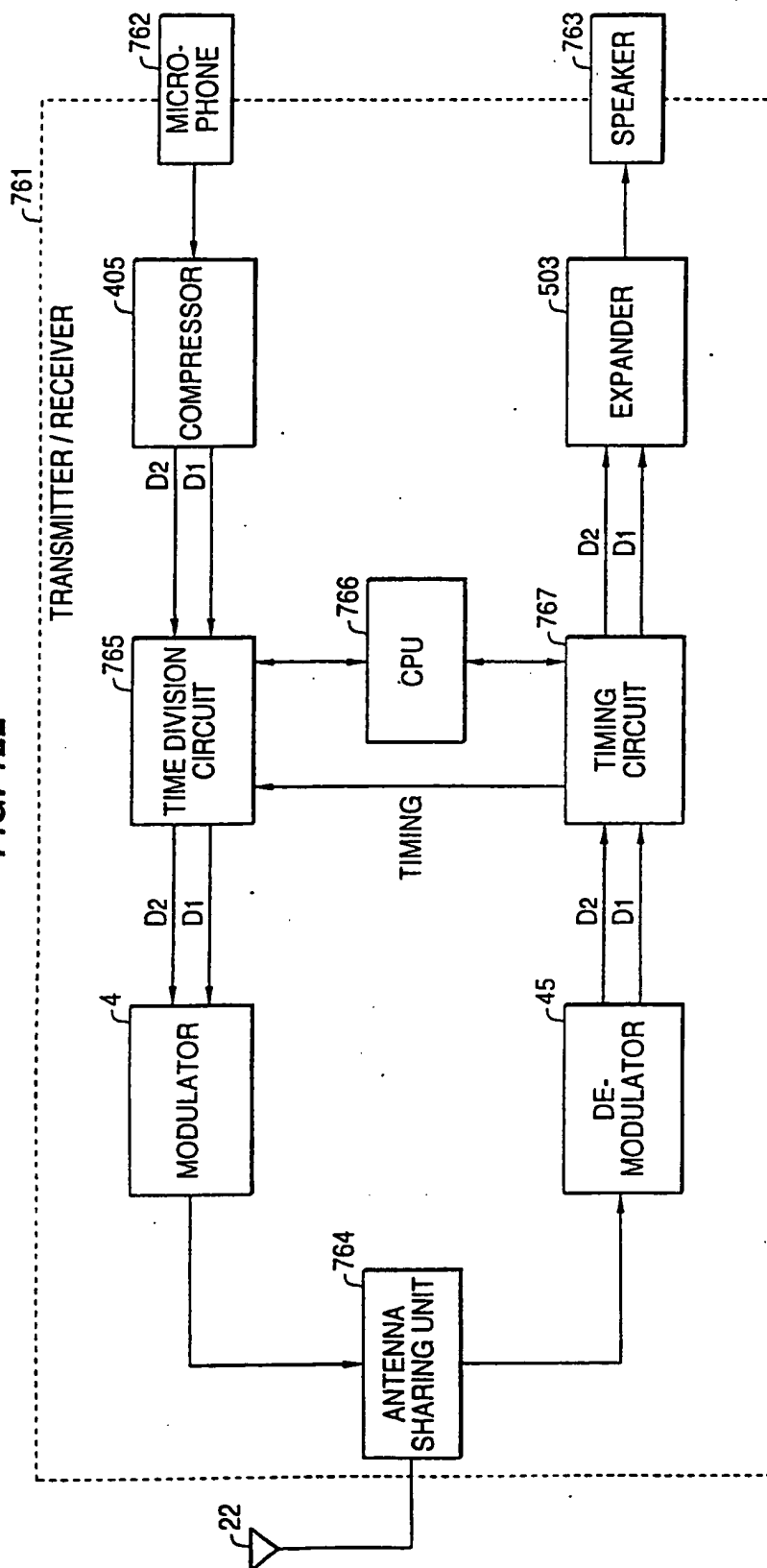
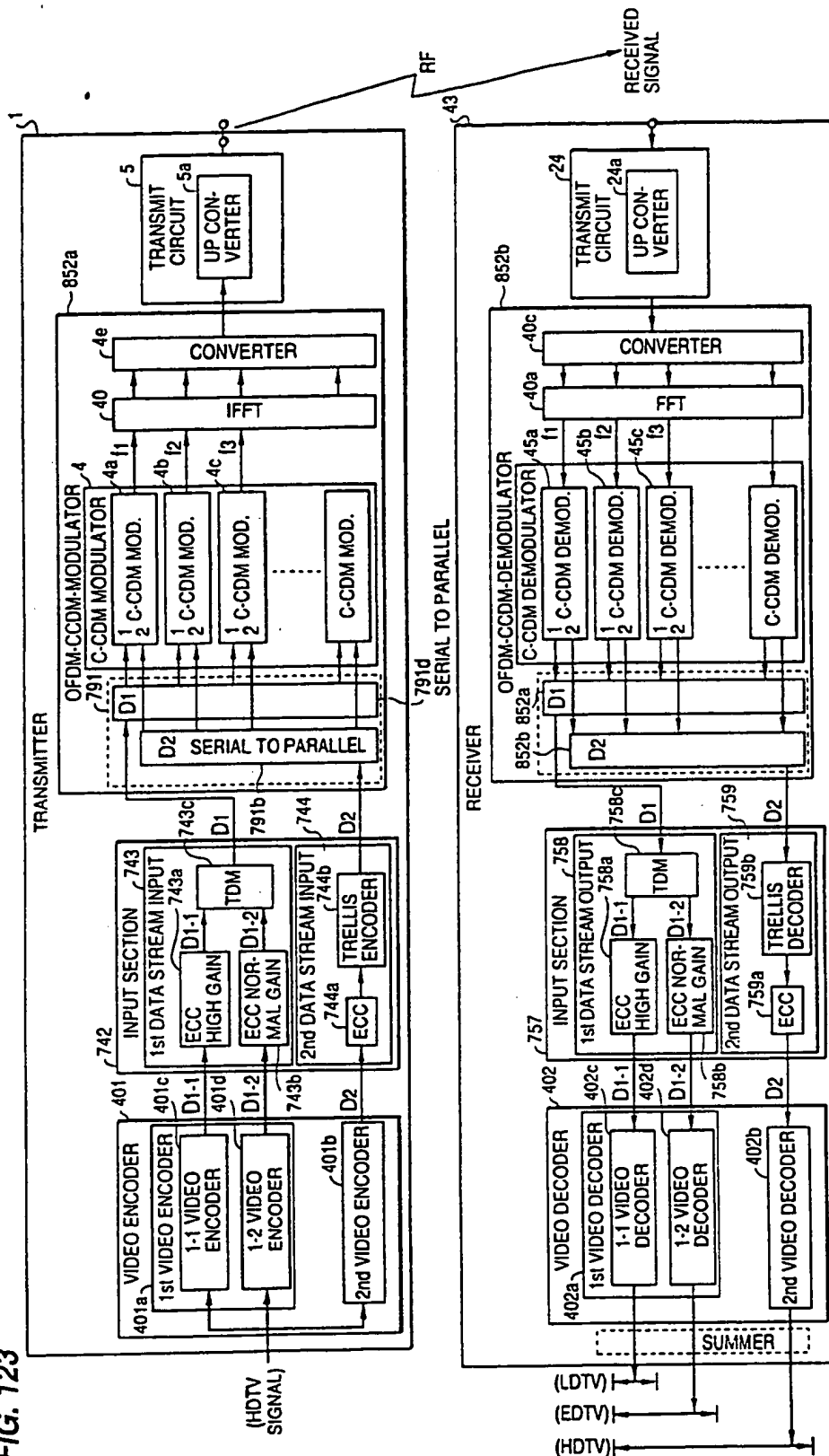


FIG. 122





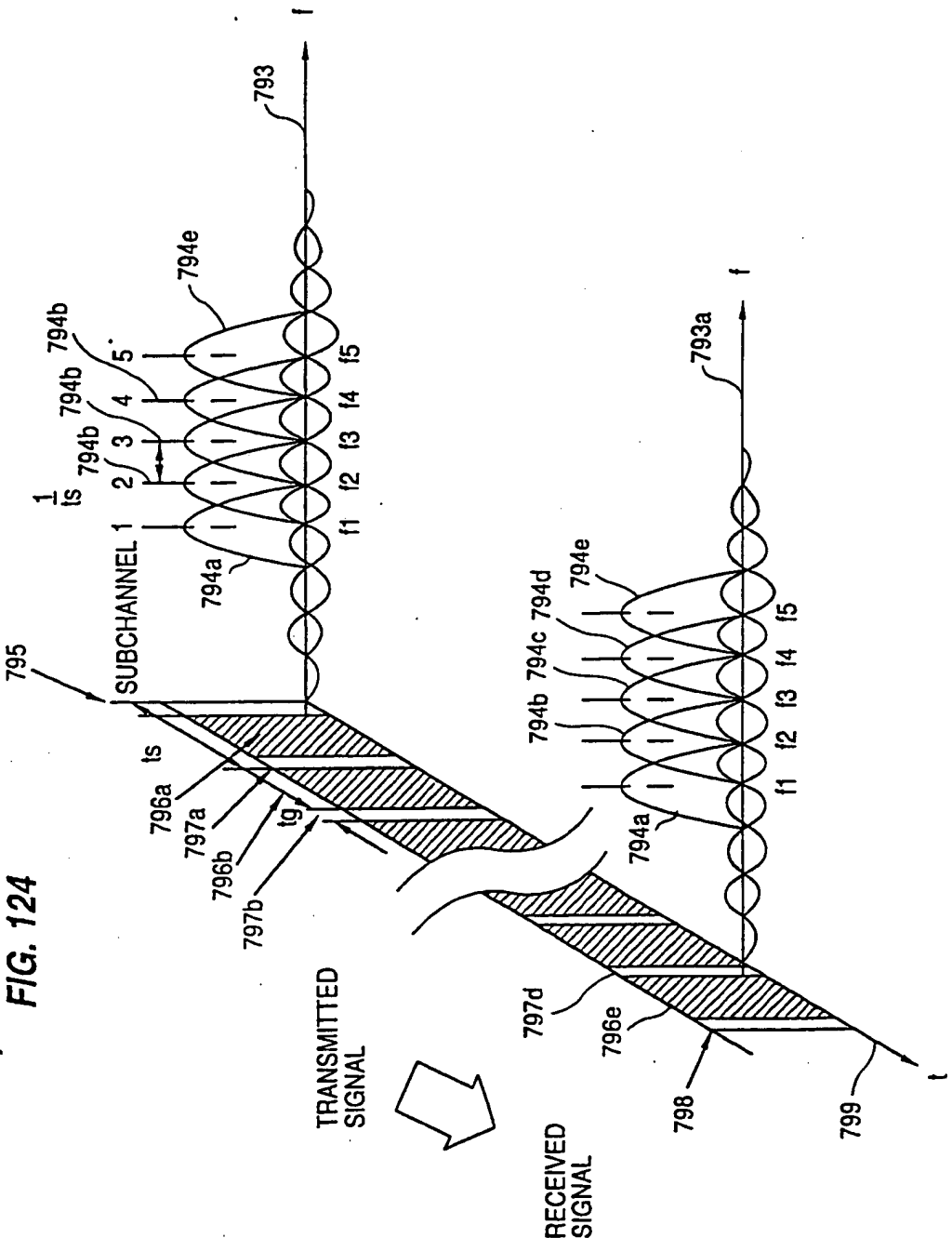


FIG. 125(a)

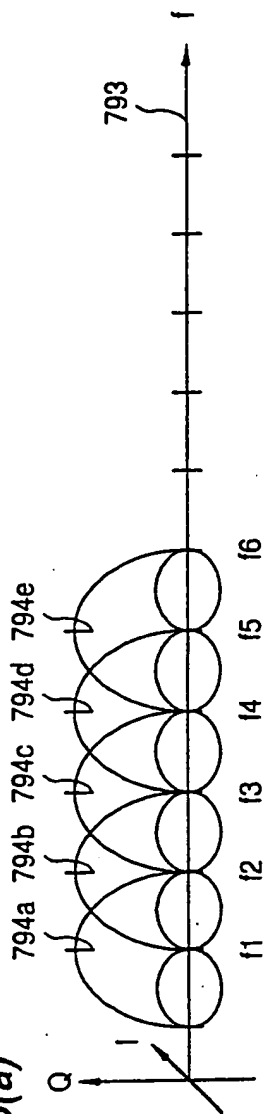
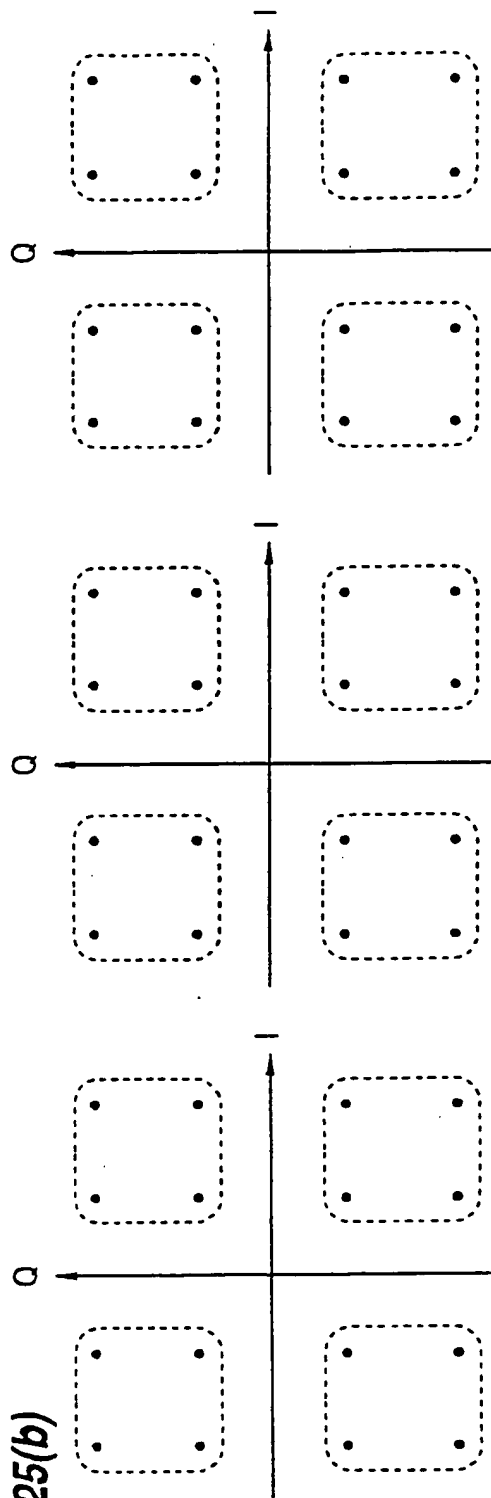
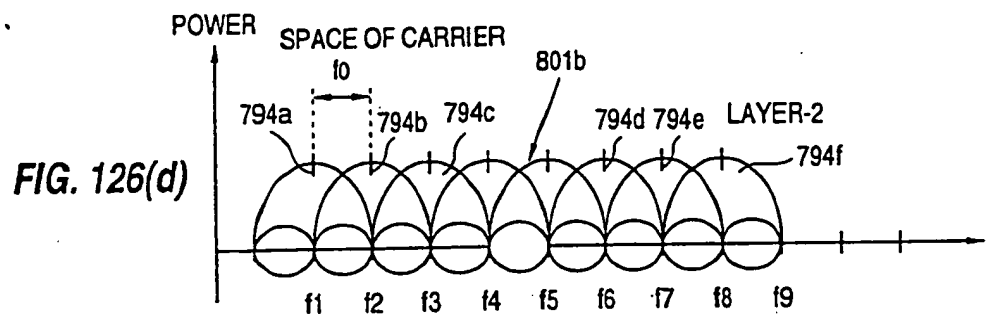
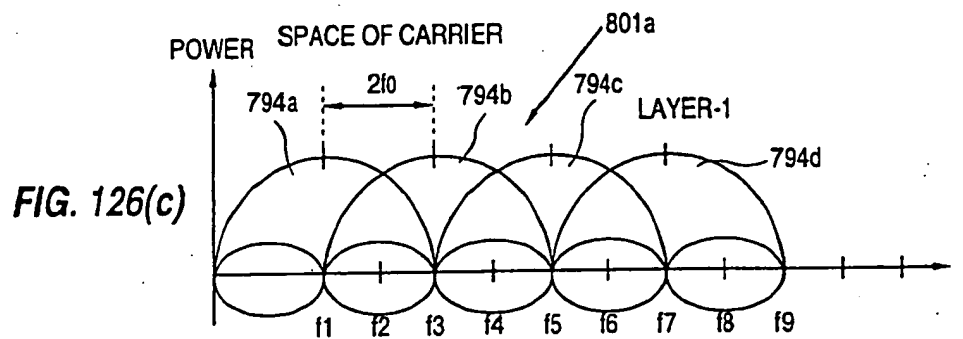
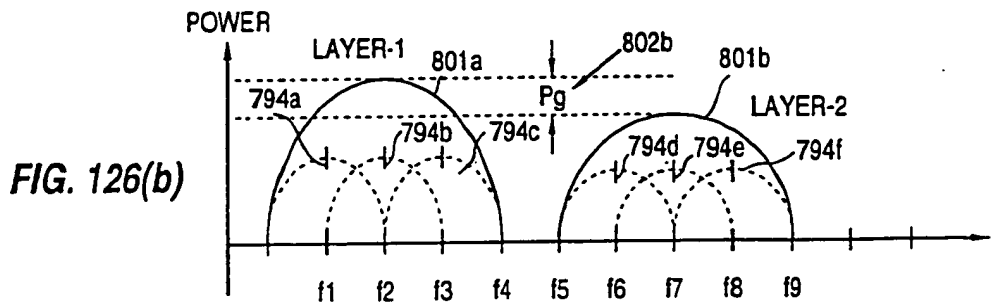
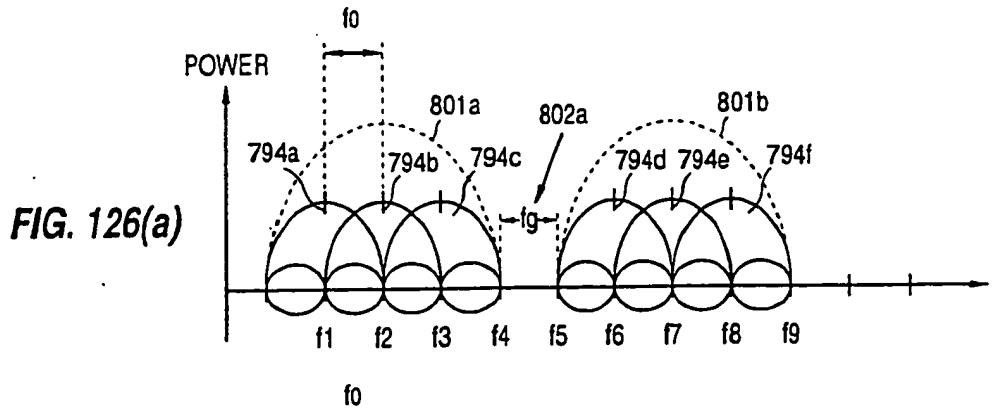


FIG. 125(b)





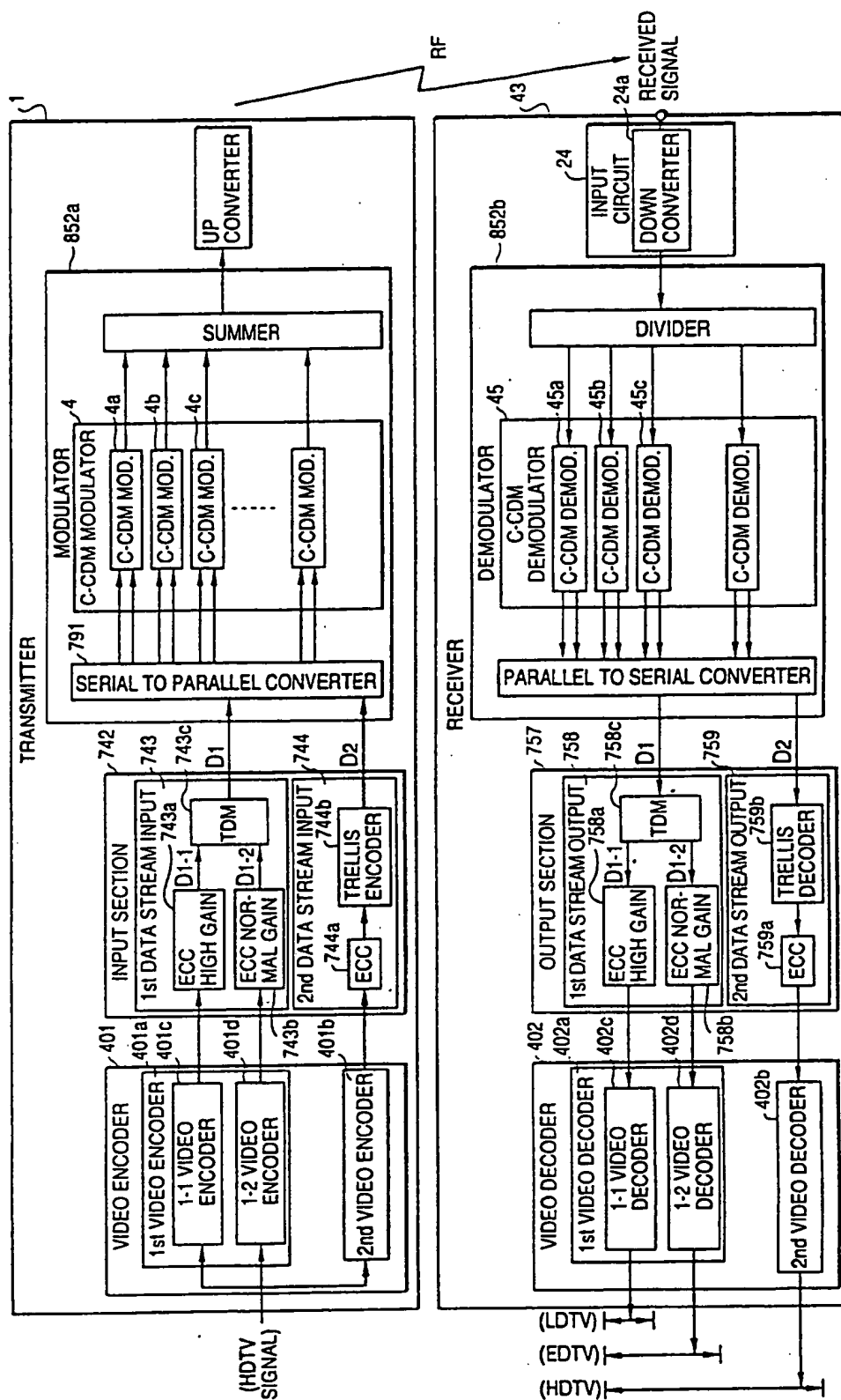


FIG. 128(a)

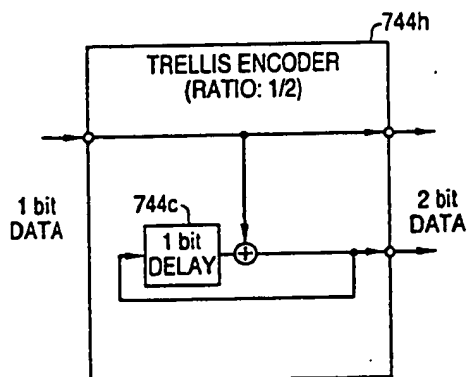


FIG. 128(d)

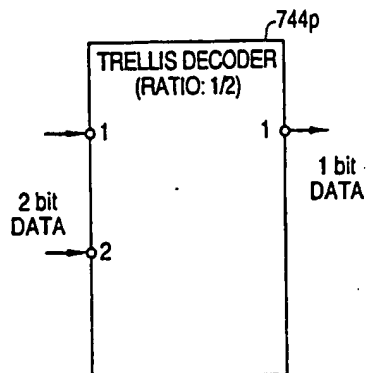


FIG. 128(b)

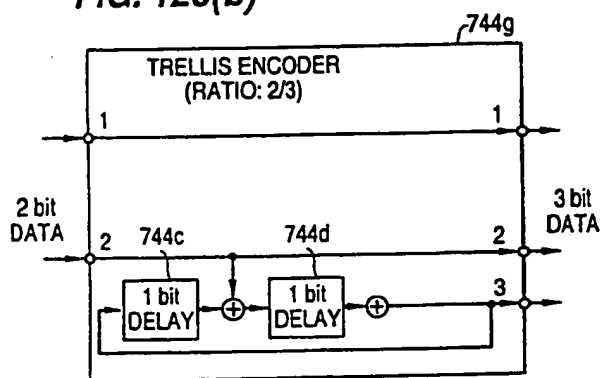


FIG. 128(e)

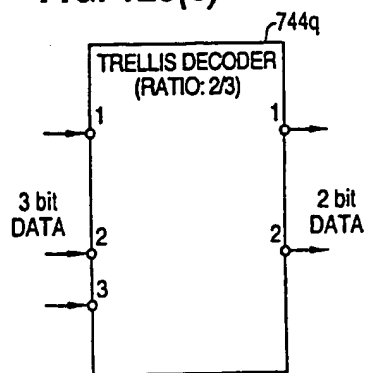


FIG. 128(c)

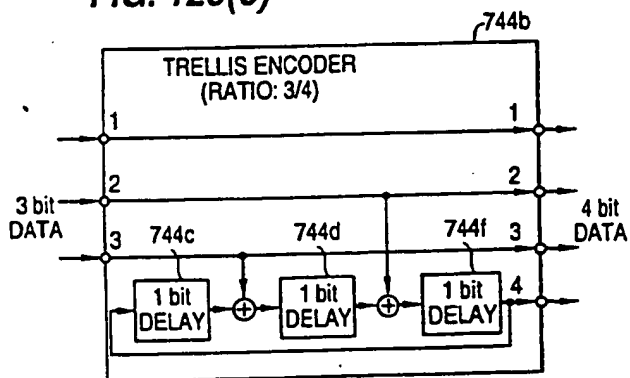


FIG. 128(f)

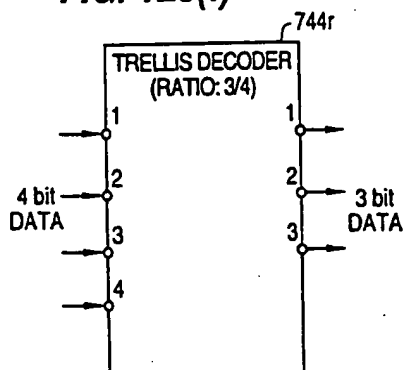


FIG. 129

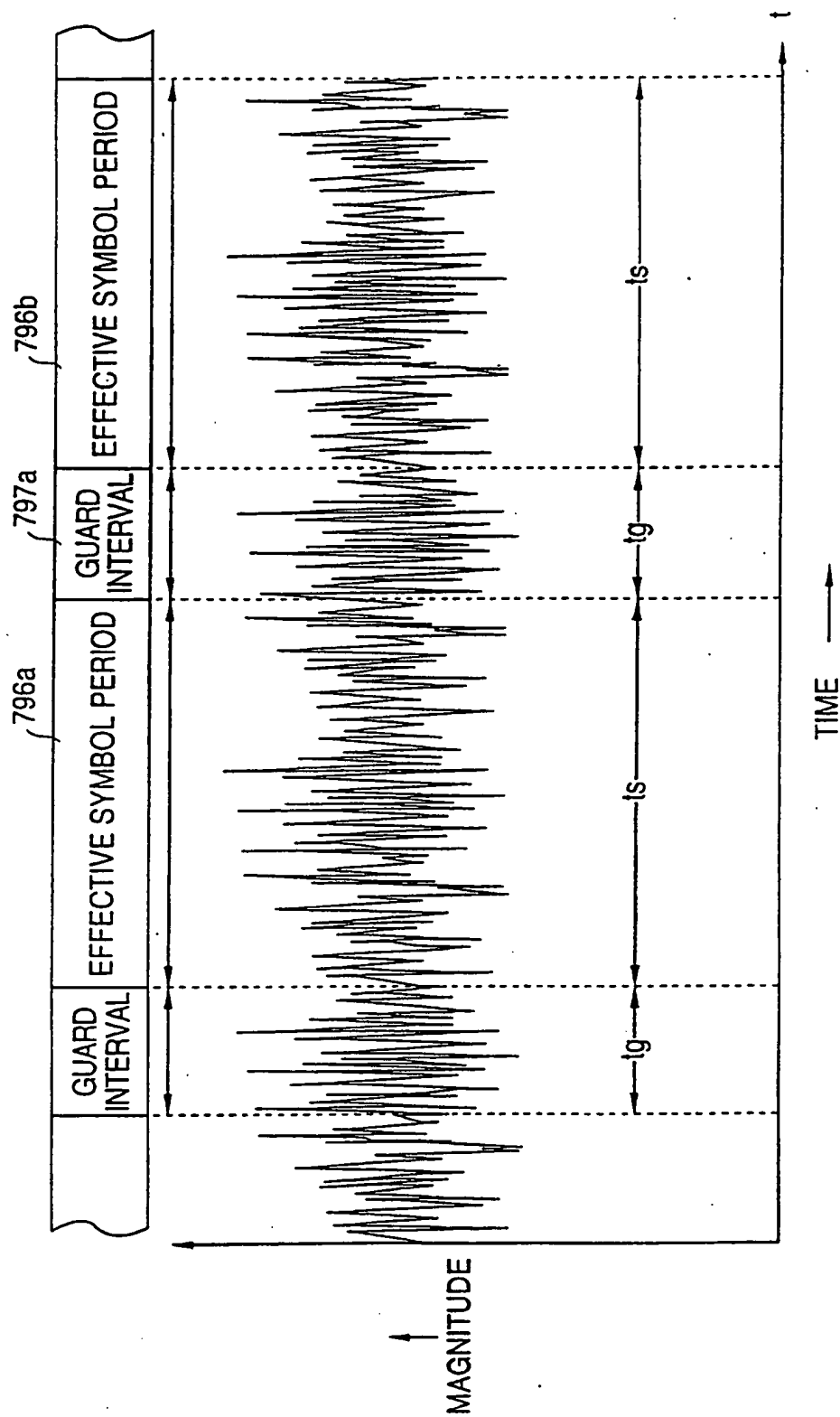


FIG. 130

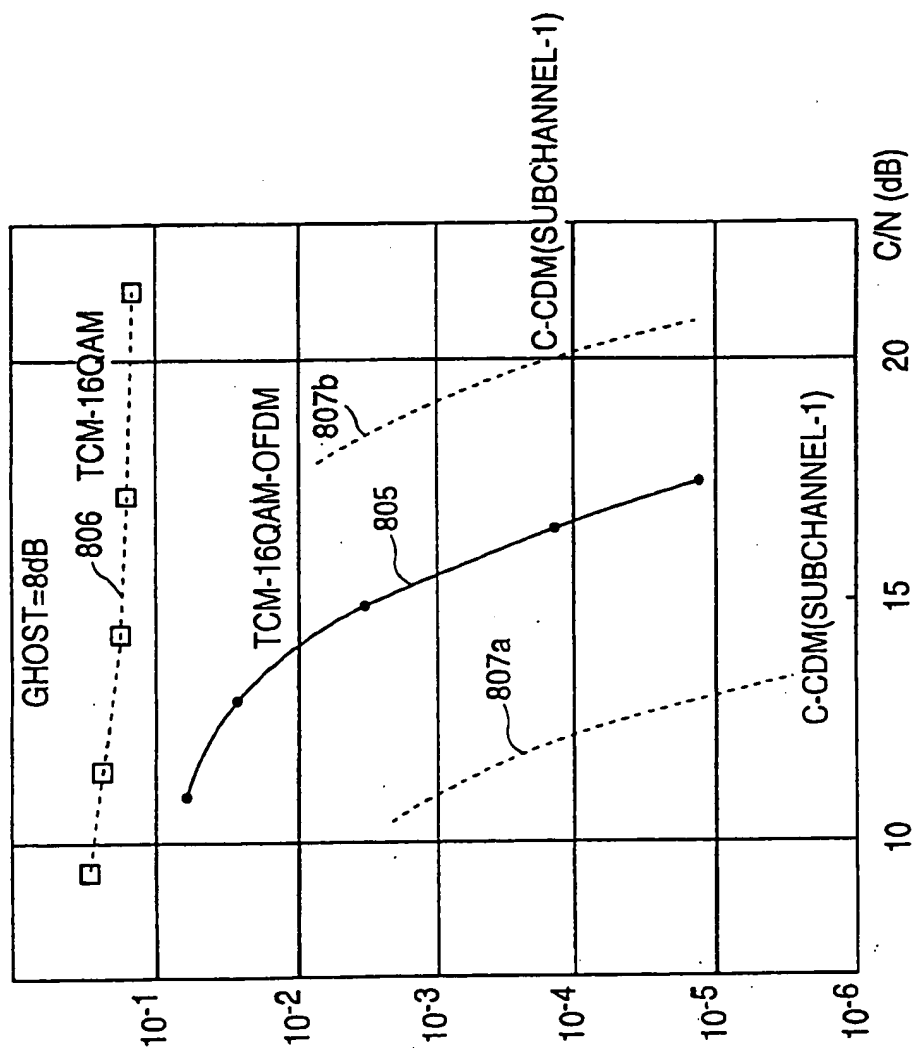
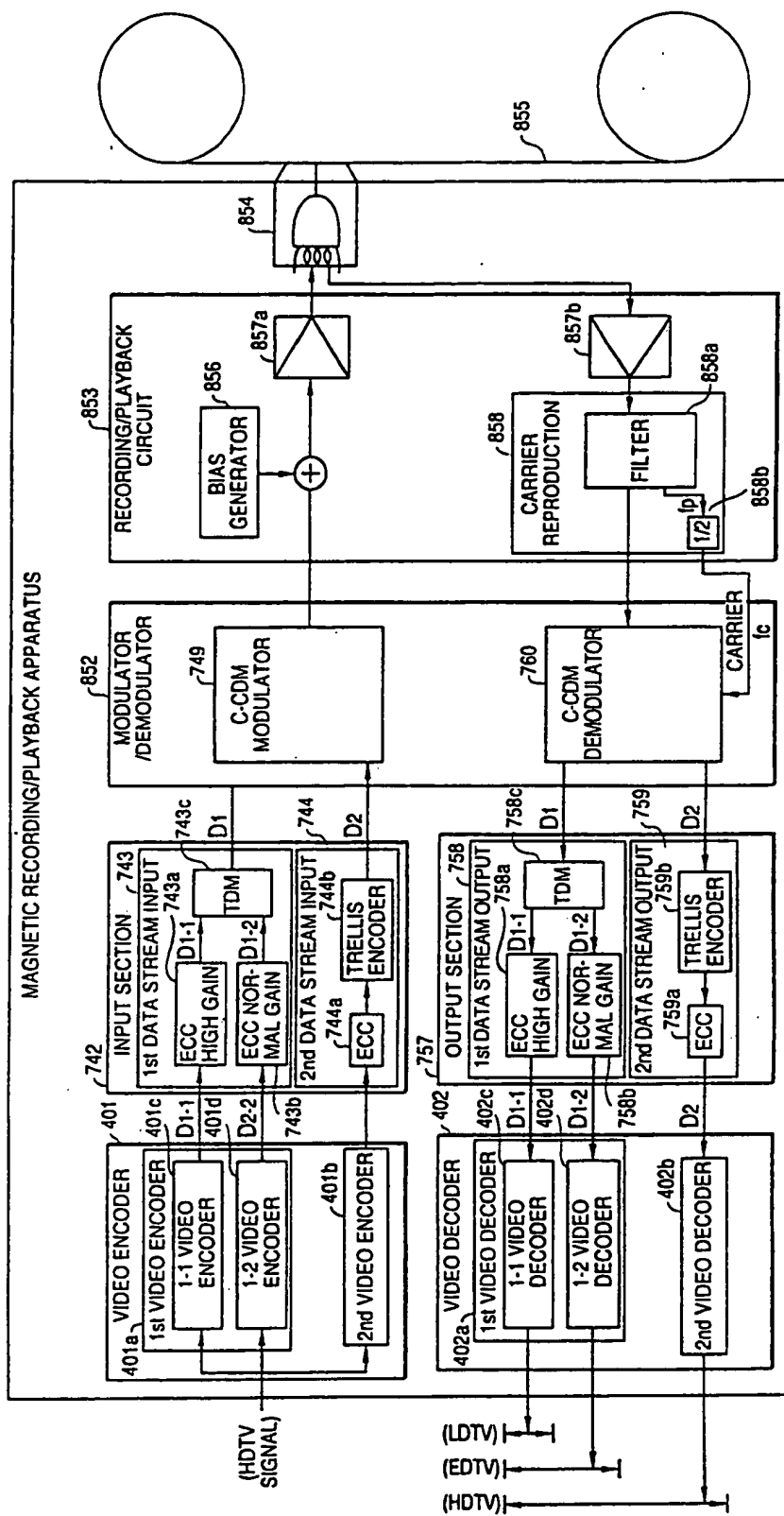
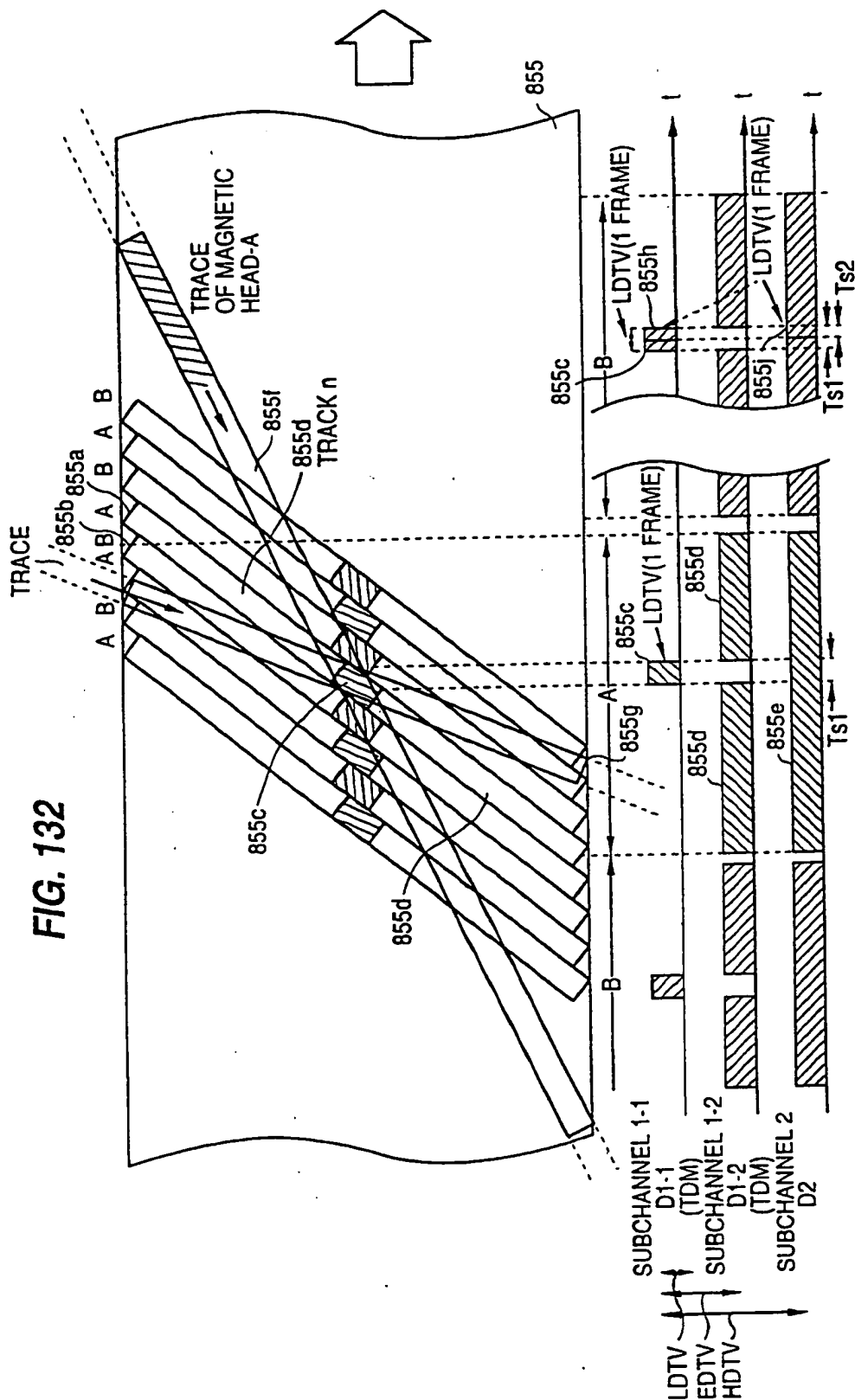


FIG. 131





[illegible]

FIG. 133

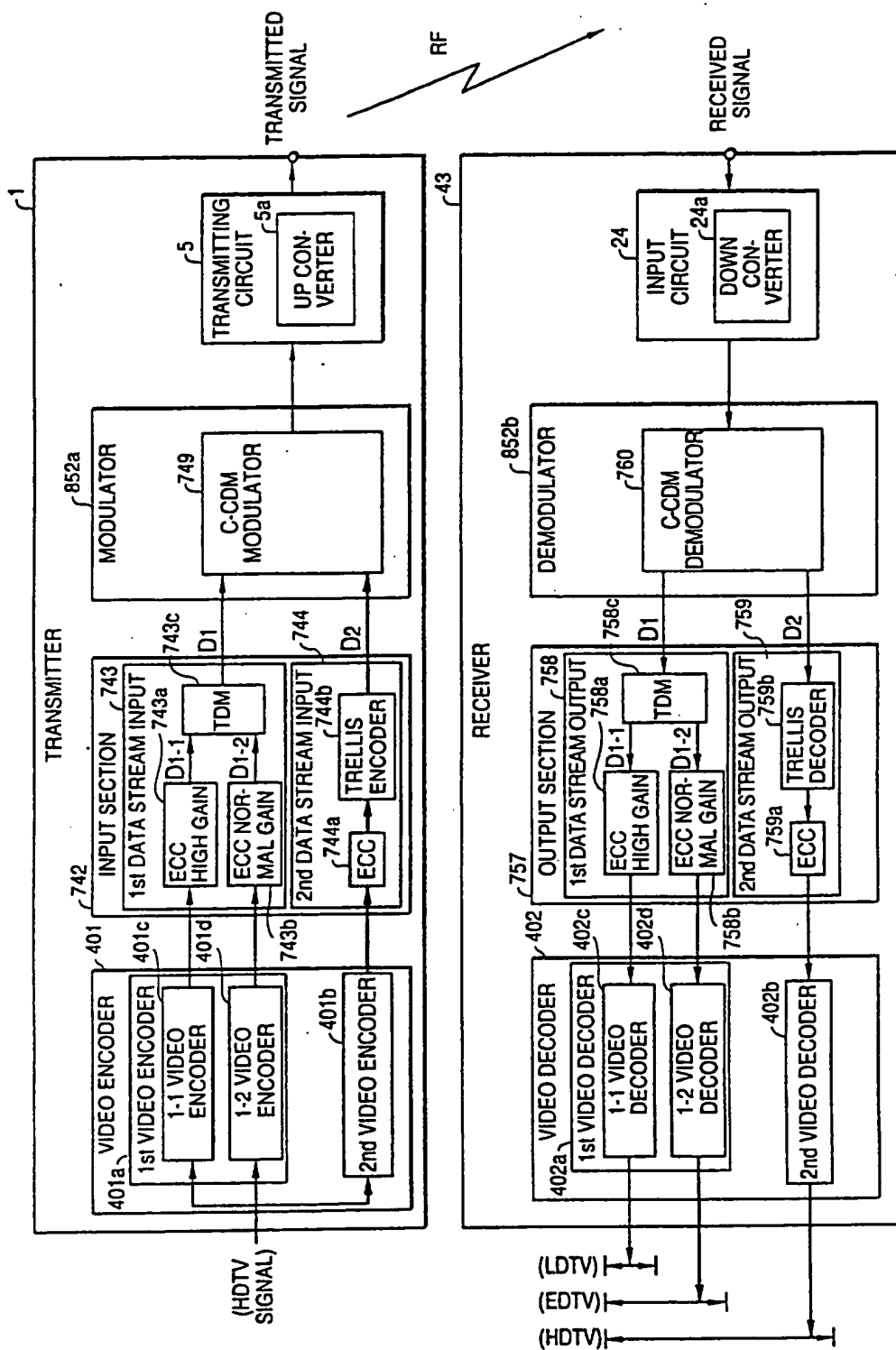


FIG. 134

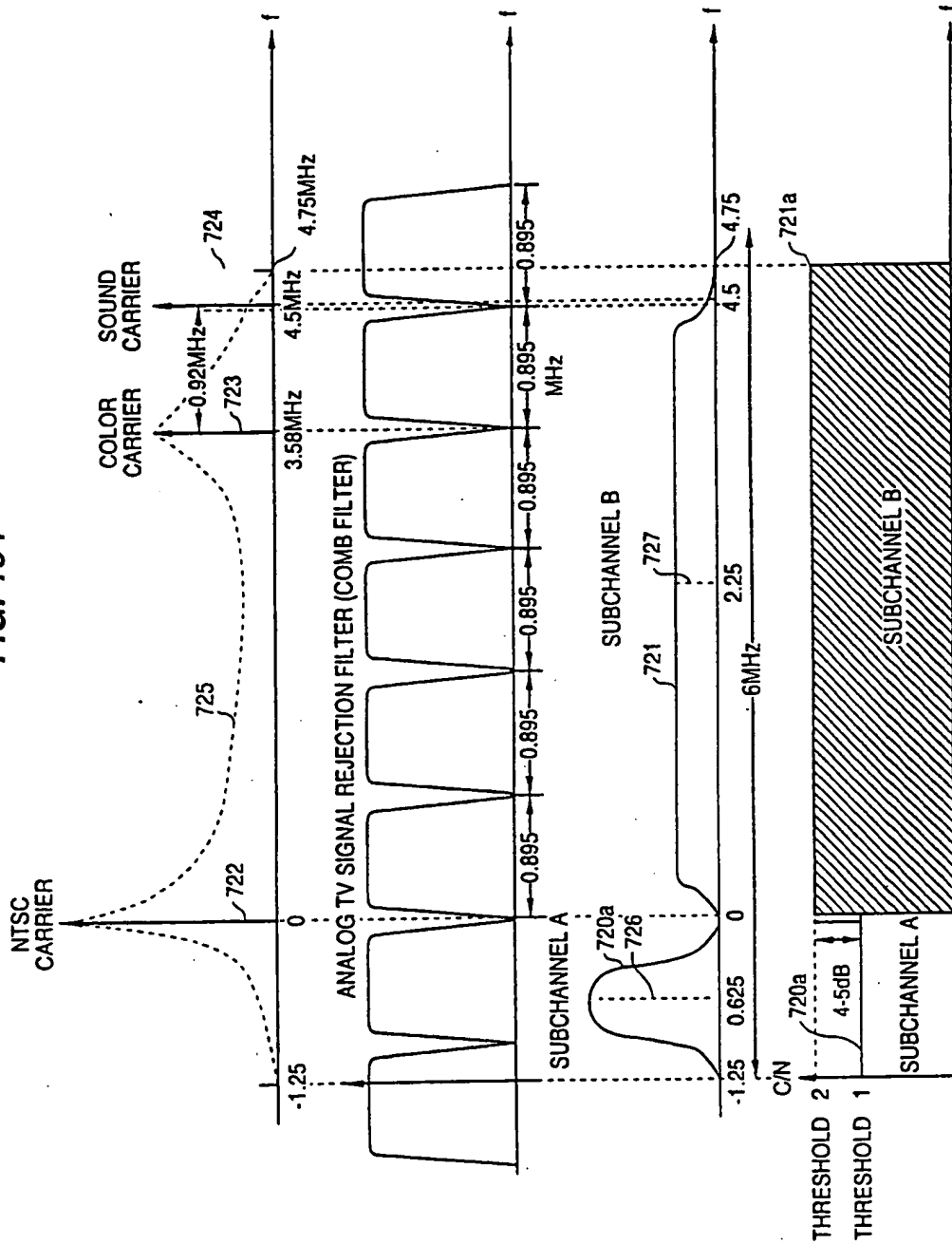


FIG. 135

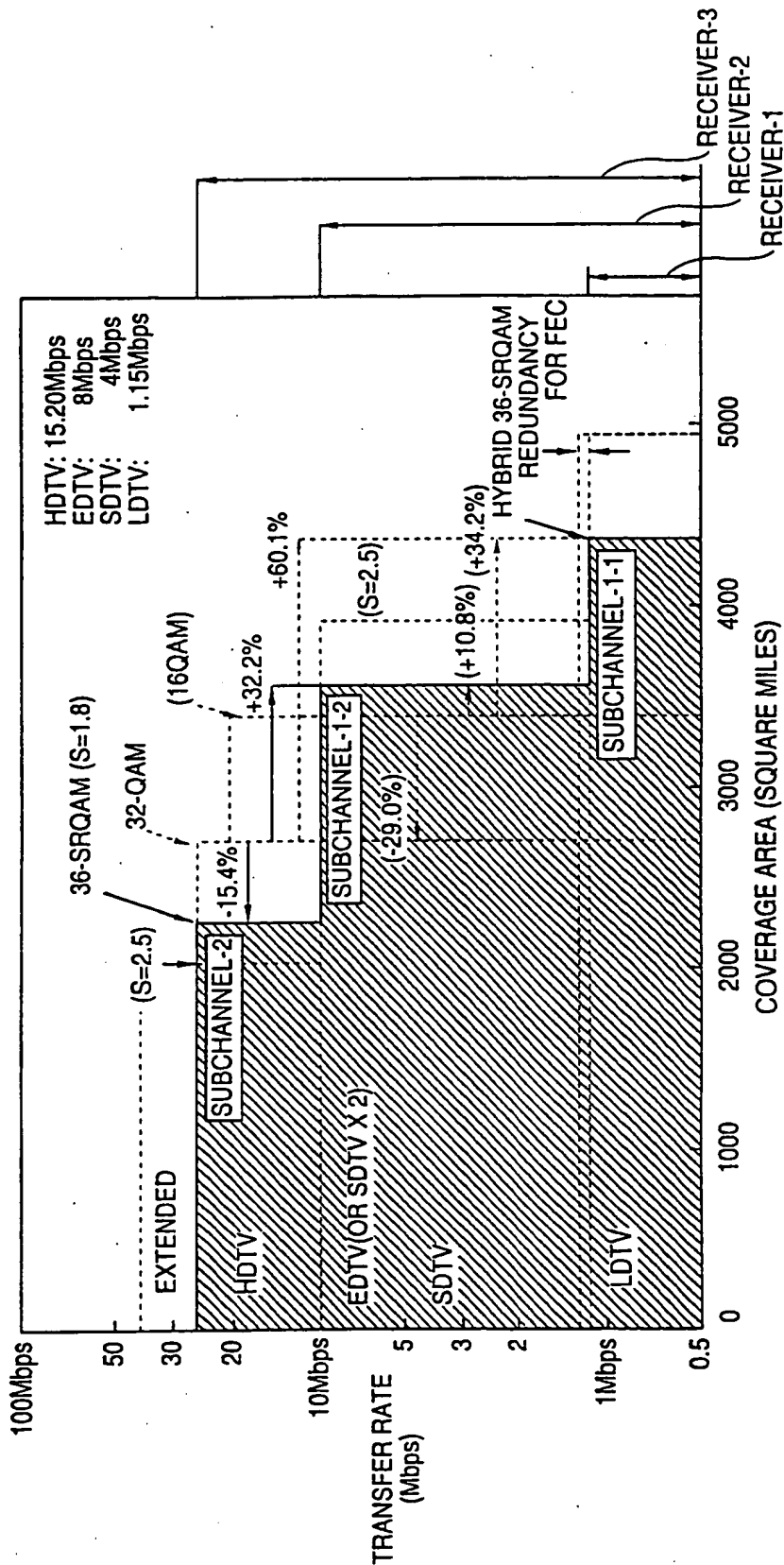


FIG. 136

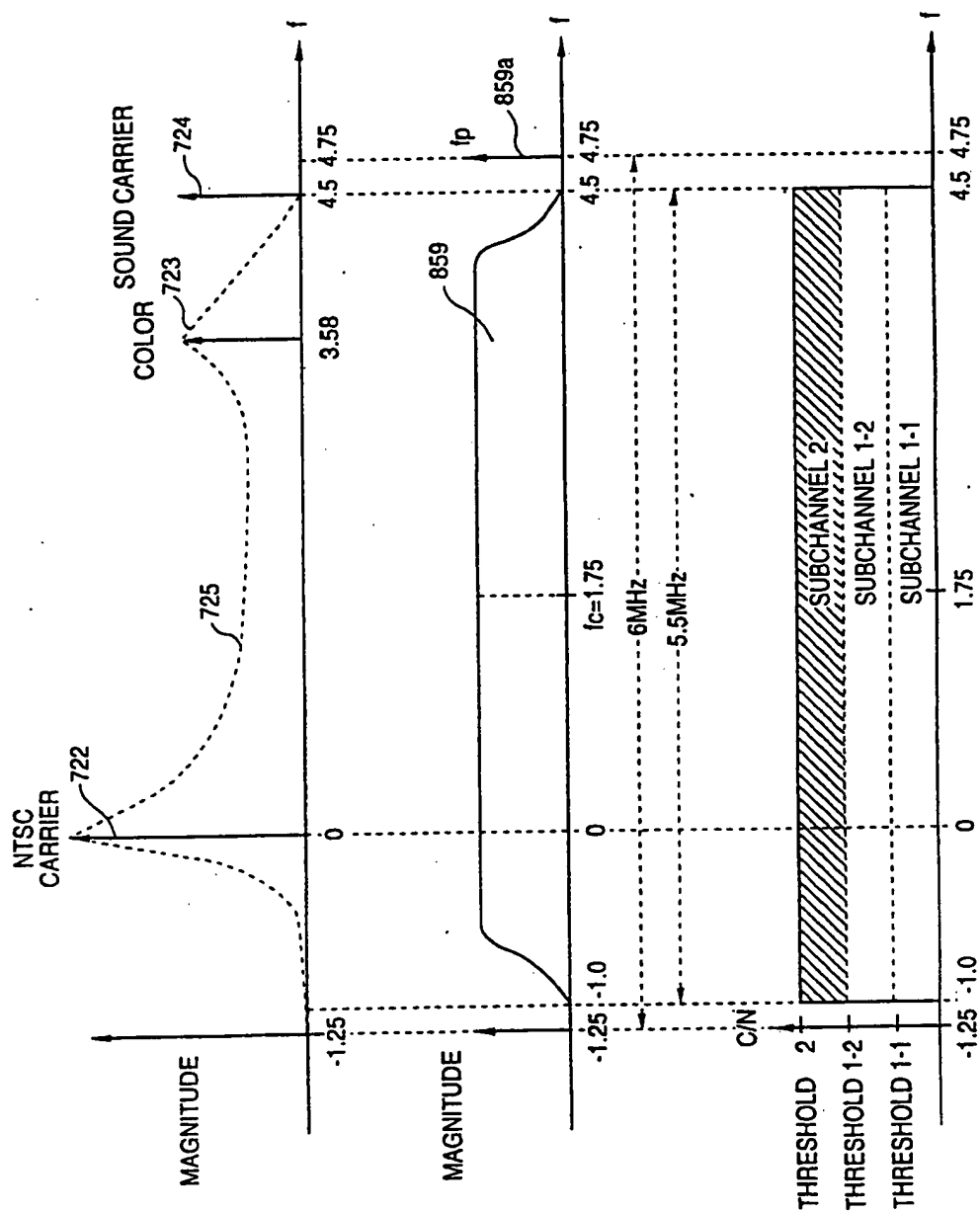


FIG. 137

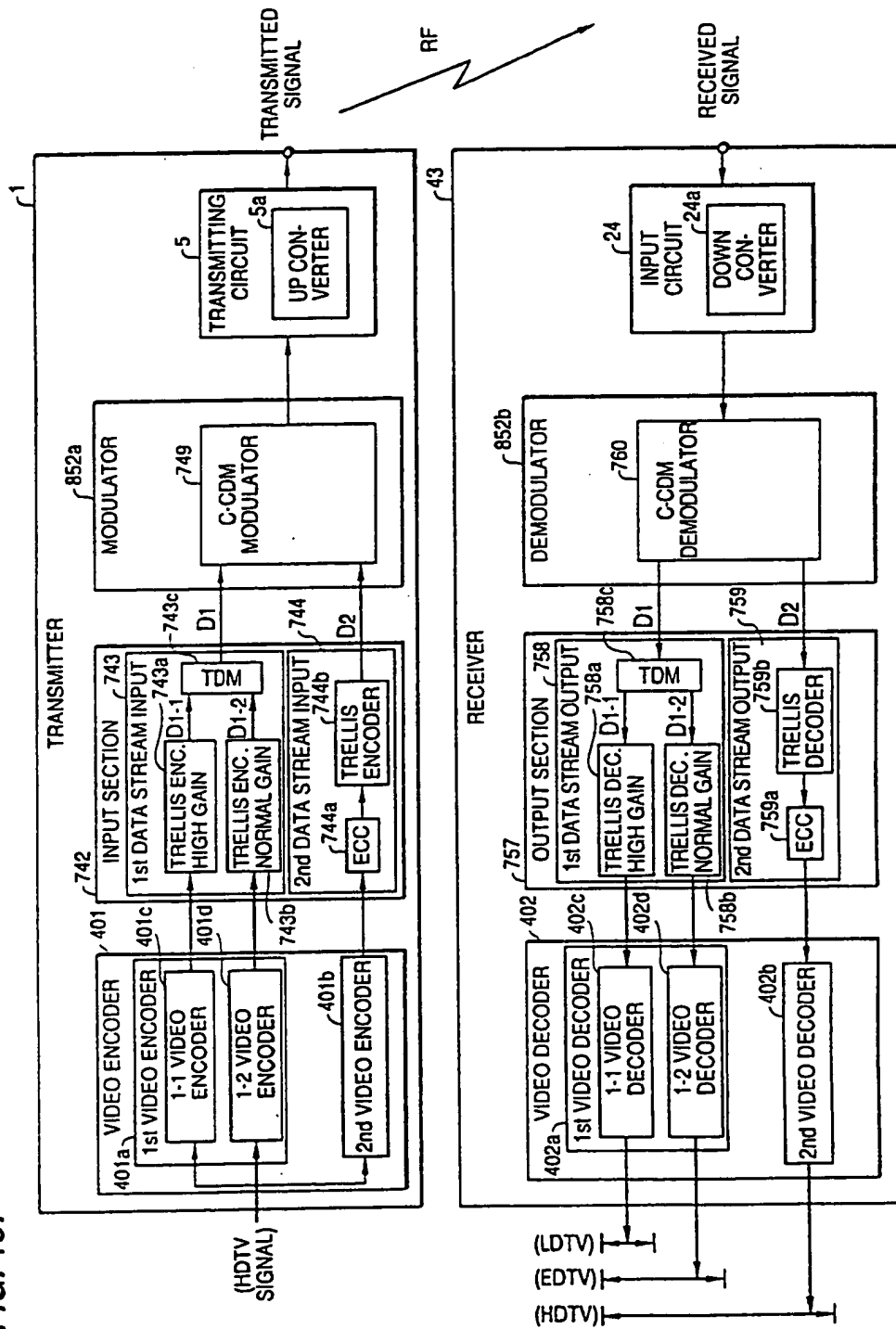


FIG. 138

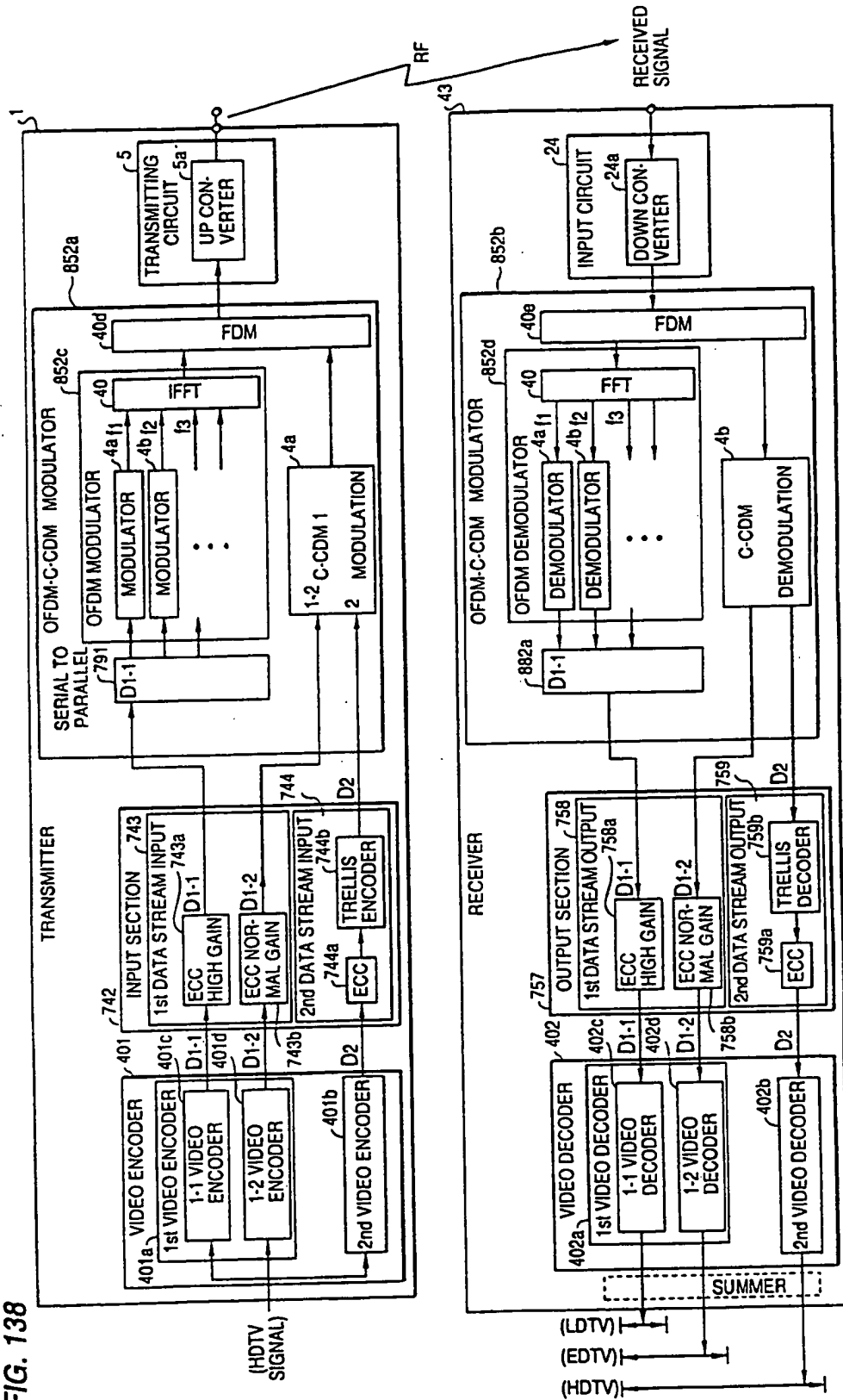
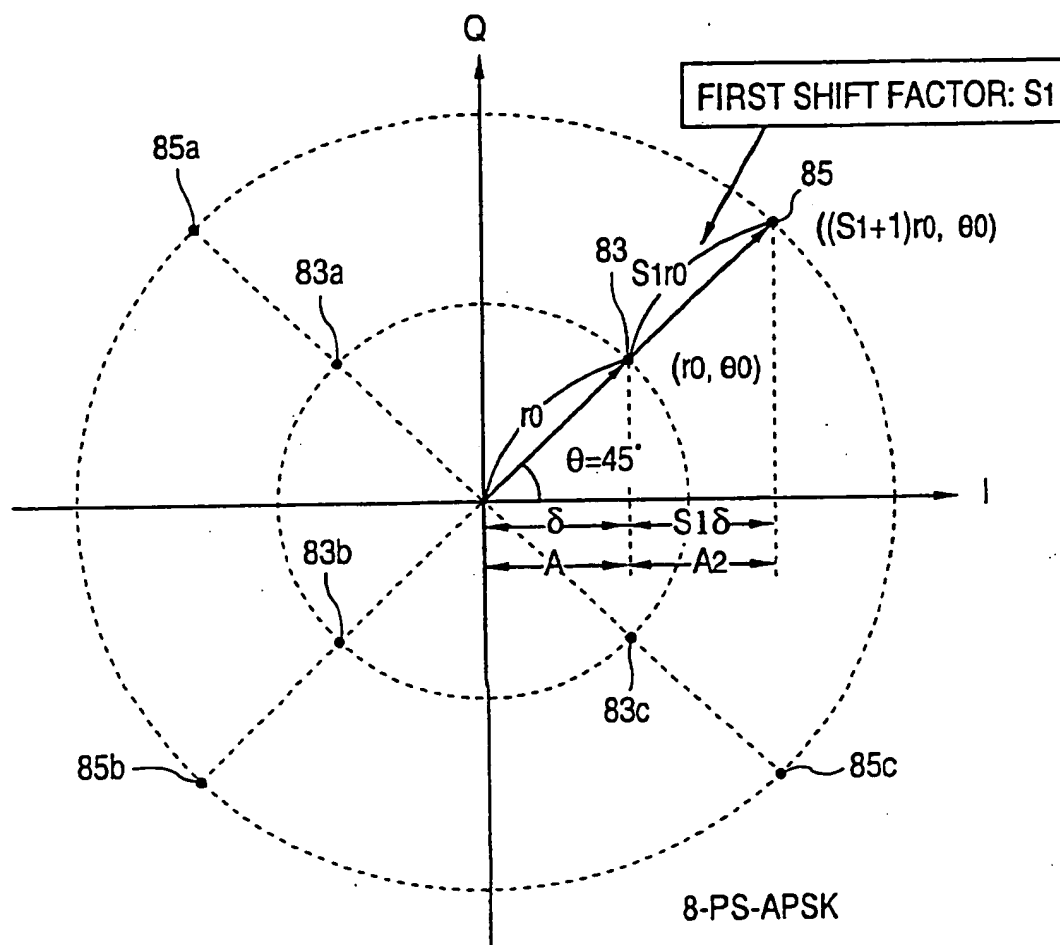


FIG. 139



0060017 100600

FIG. 140

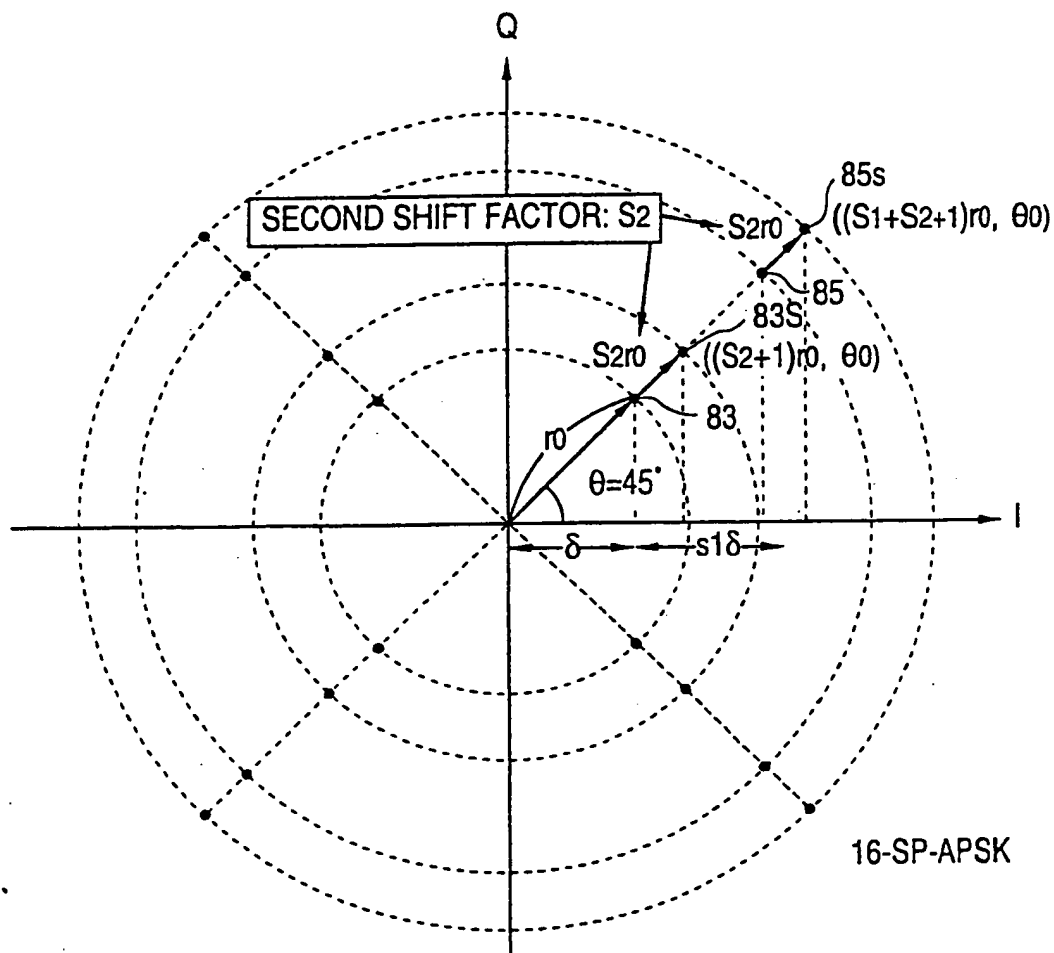


FIG. 141

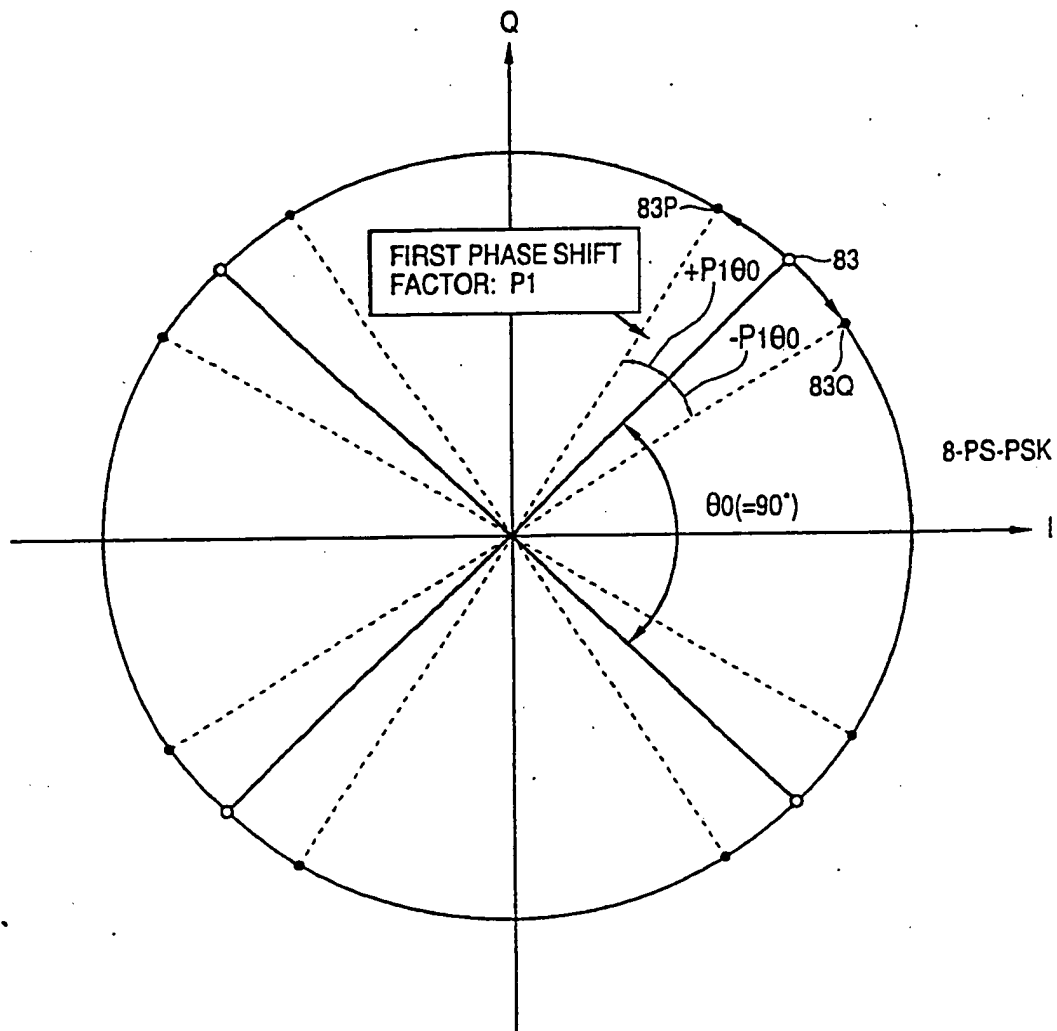
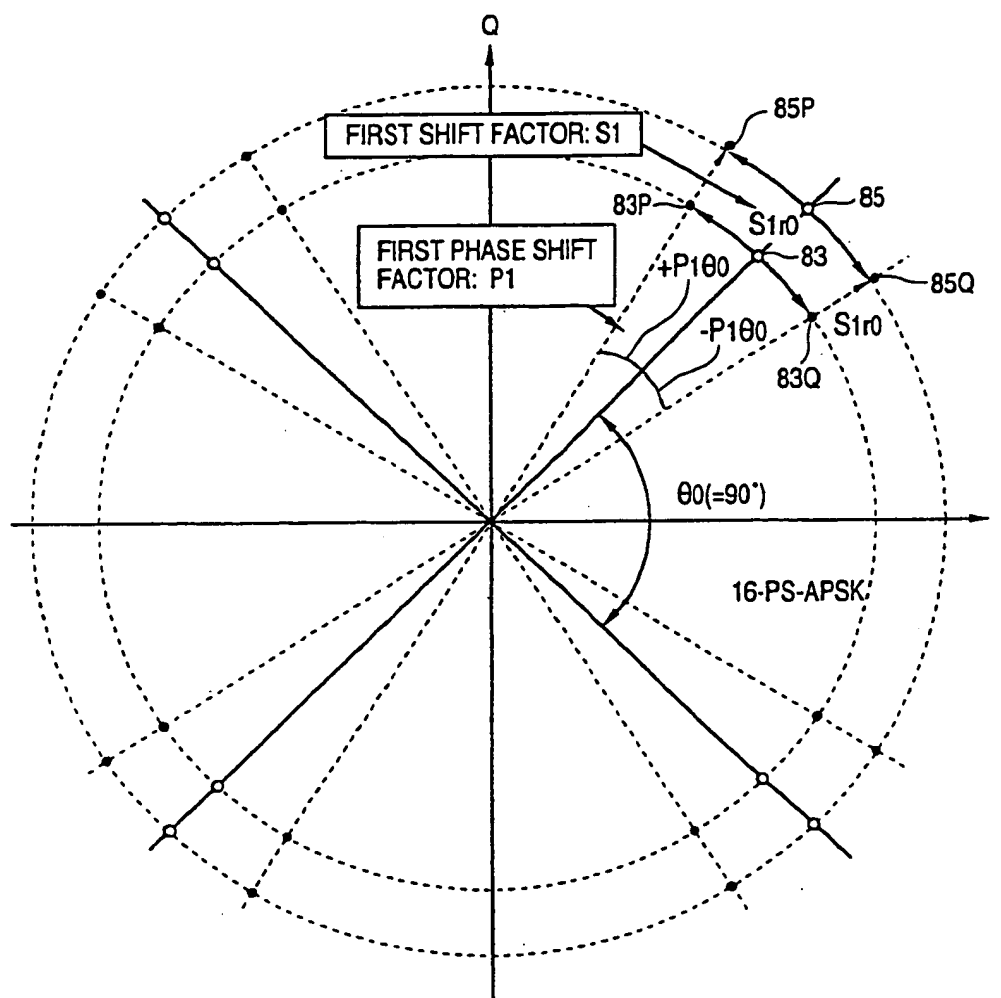
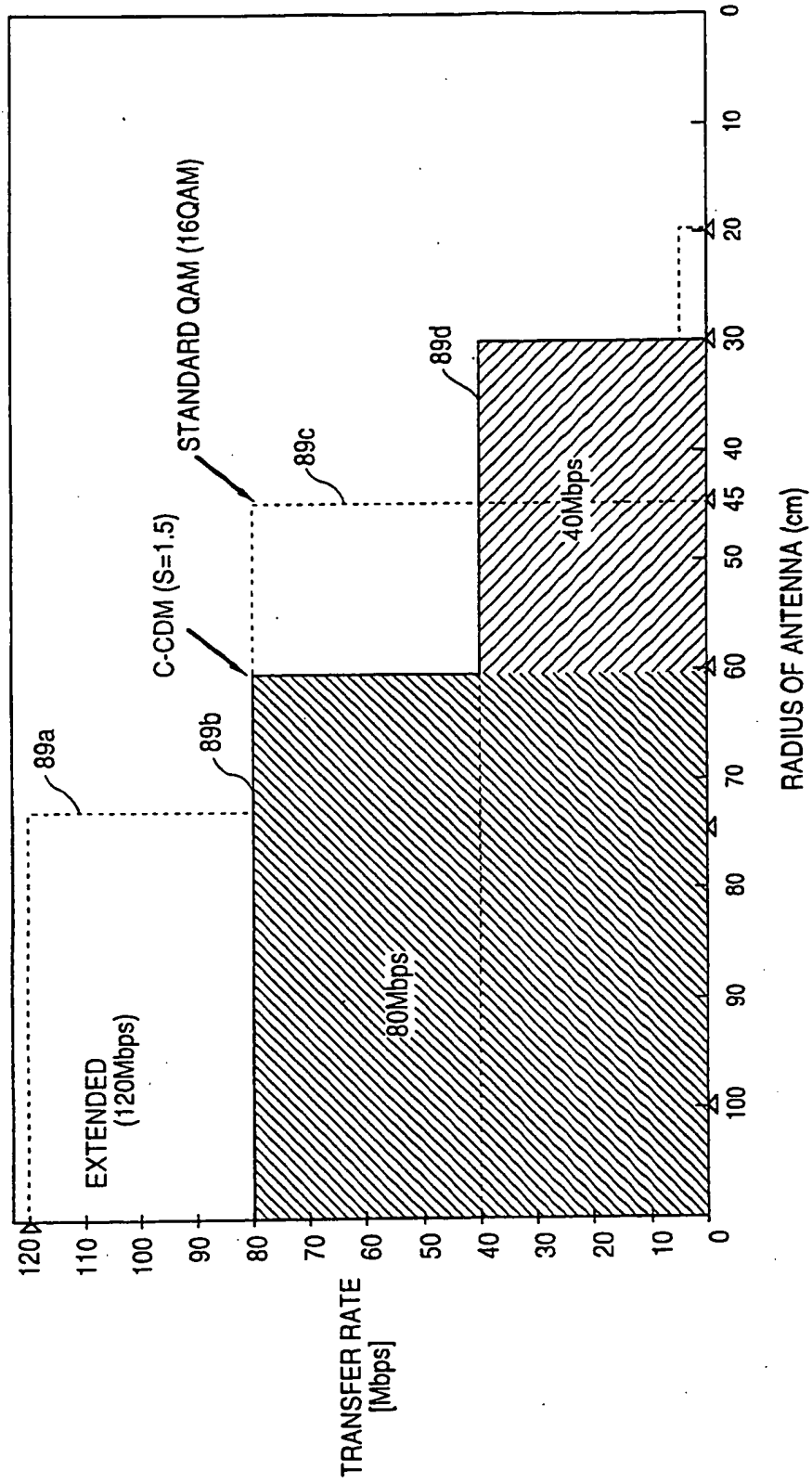


FIG. 142



000001 100000

FIG. 143



The diagram illustrates a video transmission system, divided into a **TRANSMITTER** and a **RECEIVER**.

TRANSMITTER:

- Input Section (742):** Receives an **(HDTV SIGNAL)**. It includes a **VIDEO ENCODER (401)** with a **1st VIDEO ENCODER (401c)** and a **2nd VIDEO ENCODER (401b)**. The 1st encoder has **1-1 VIDEO ENCODER (401d)** and **1-2 VIDEO ENCODER (401e)** sub-blocks. The output of the 1st encoder is the **1st DATA STREAM INPUT (743)**, which passes through an **ECC (743a)**, **HIGH GAIN (743b)**, and **TDM (743c)** blocks. The output of the 2nd encoder is the **2nd DATA STREAM INPUT (744)**, which passes through an **ECC (744a)** and **MAL GAIN (744b)** blocks.
- Serial to Parallel (791a):** A **D2 SERIAL TO PARALLEL** block that takes the two data streams and outputs **D1** and **D2** signals.
- Weighted OFDM-Modulator (4):** A **WEIGHTED OFDM-MODULATOR** block that receives **D1** and **D2**. It contains multiple **MOD.** (modulator) blocks (4a1f, 4b1f, 4c1f, 4d1f, 4e1f, 4f1f) and an **IFFT (40)** block.
- D/A Converter (4e):** A **D/A CONVERTER** block that receives the output of the modulator.
- Transmit Circuit (5a):** An **UP CON-VERTER** block that receives the output of the D/A converter and outputs an **RF** (Radio Frequency) signal.

RECEIVER:

- Input Circuit (24a):** An **INPUT CIRCUIT** block that receives a **RECEIVED SIGNAL**.
- A/D Converter (40c):** An **A/D CONVERTER** block that receives the output of the input circuit.
- FFT (40a):** An **FFT** (Fast Fourier Transform) block that receives the output of the A/D converter.
- Weighted OFDM-Demodulator (45):** A **WEIGHTED OFDM-DEMODULATOR** block that receives the output of the FFT. It contains multiple **DEMOD.** (demodulator) blocks (45a1f, 45b1f, 45c1f, 45d1f, 45e1f, 45f1f) and a **D2** block.
- Parallel to Serial (791b):** A **D2** block that receives the output of the demodulator and outputs **D1** and **D2** signals.
- Output Section (757):** Receives **D1** and **D2**. It includes an **OUTPUT SECTION (758)** with an **ECC (758a)**, **HIGH GAIN (758b)**, and **TDM (758c)** blocks. The output of the 1st encoder is the **1st DATA STREAM OUTPUT (758d)**, which passes through an **ECC (758e)**, **HIGH GAIN (758f)**, and **TDM (758g)** blocks. The output of the 2nd encoder is the **2nd DATA STREAM OUTPUT (759)**, which passes through an **ECC (759a)** and **MAL GAIN (759b)** blocks.
- Video Decoder (402):** A **VIDEO DECODER** block that receives the output of the output section. It includes a **1st VIDEO DECODER (402c)** and a **2nd VIDEO DECODER (402b)**. The 1st decoder has **1-1 VIDEO DECODER (402d)** and **1-2 VIDEO DECODER (402e)** sub-blocks. The output of the 1st decoder is the **1st DATA STREAM OUTPUT (759a)**, which passes through an **ECC (759b)**, **HIGH GAIN (759c)**, and **TDM (759d)** blocks. The output of the 2nd decoder is the **2nd DATA STREAM OUTPUT (759e)**, which passes through an **ECC (759f)** and **MAL GAIN (759g)** blocks.
- Summer:** A **SUMMER** block that receives the output of the 1st and 2nd video decoders and outputs the final **(HDTV)** signal.

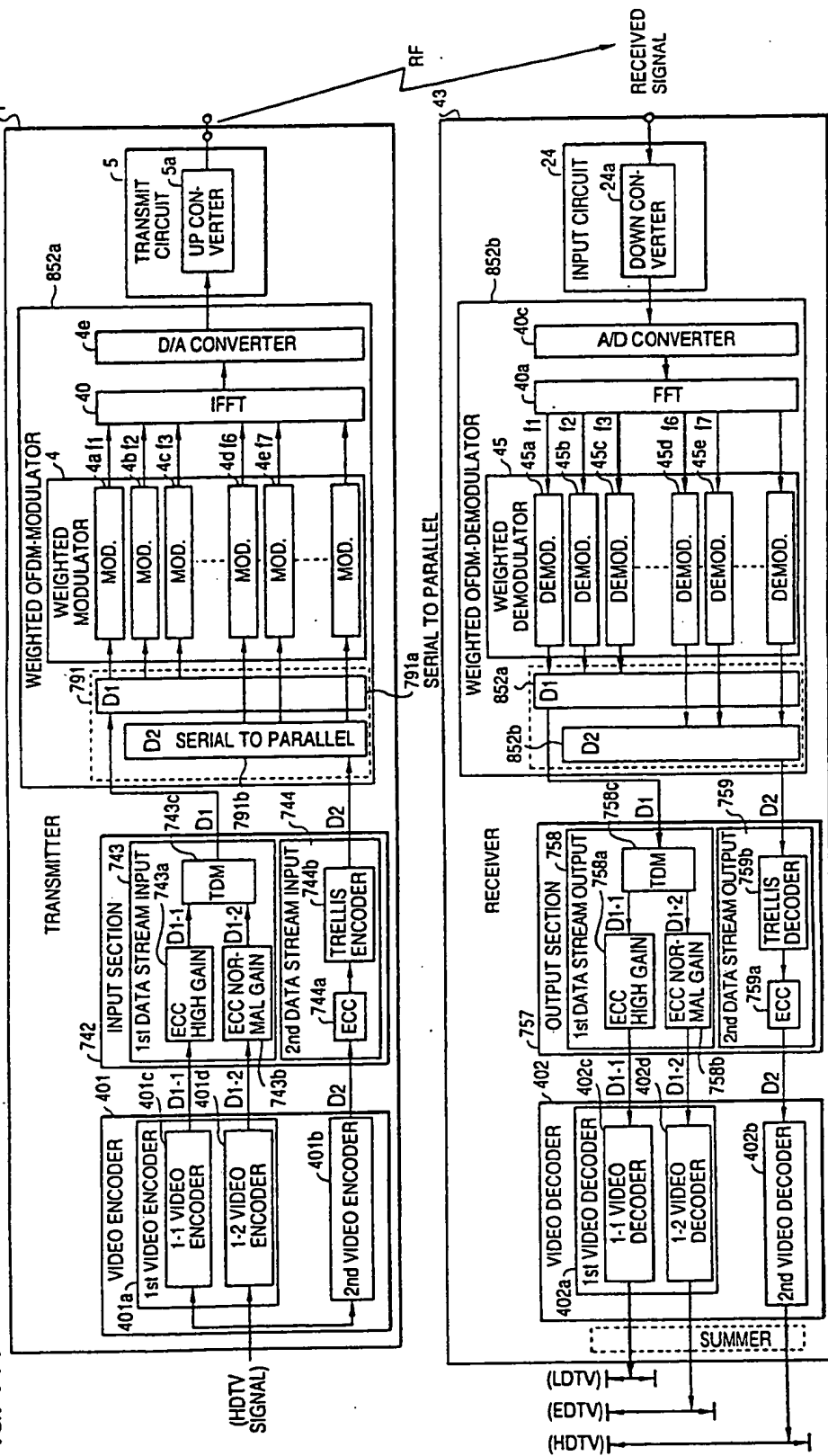


FIG. 145(a)

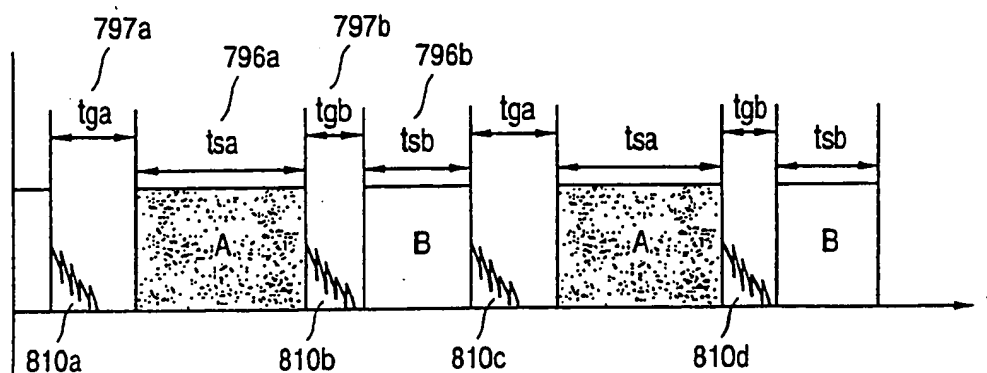


FIG. 145(b)

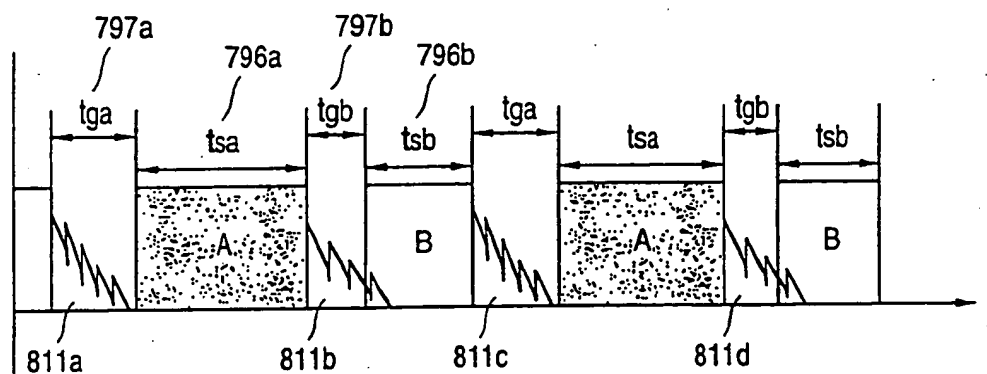


FIG. 146

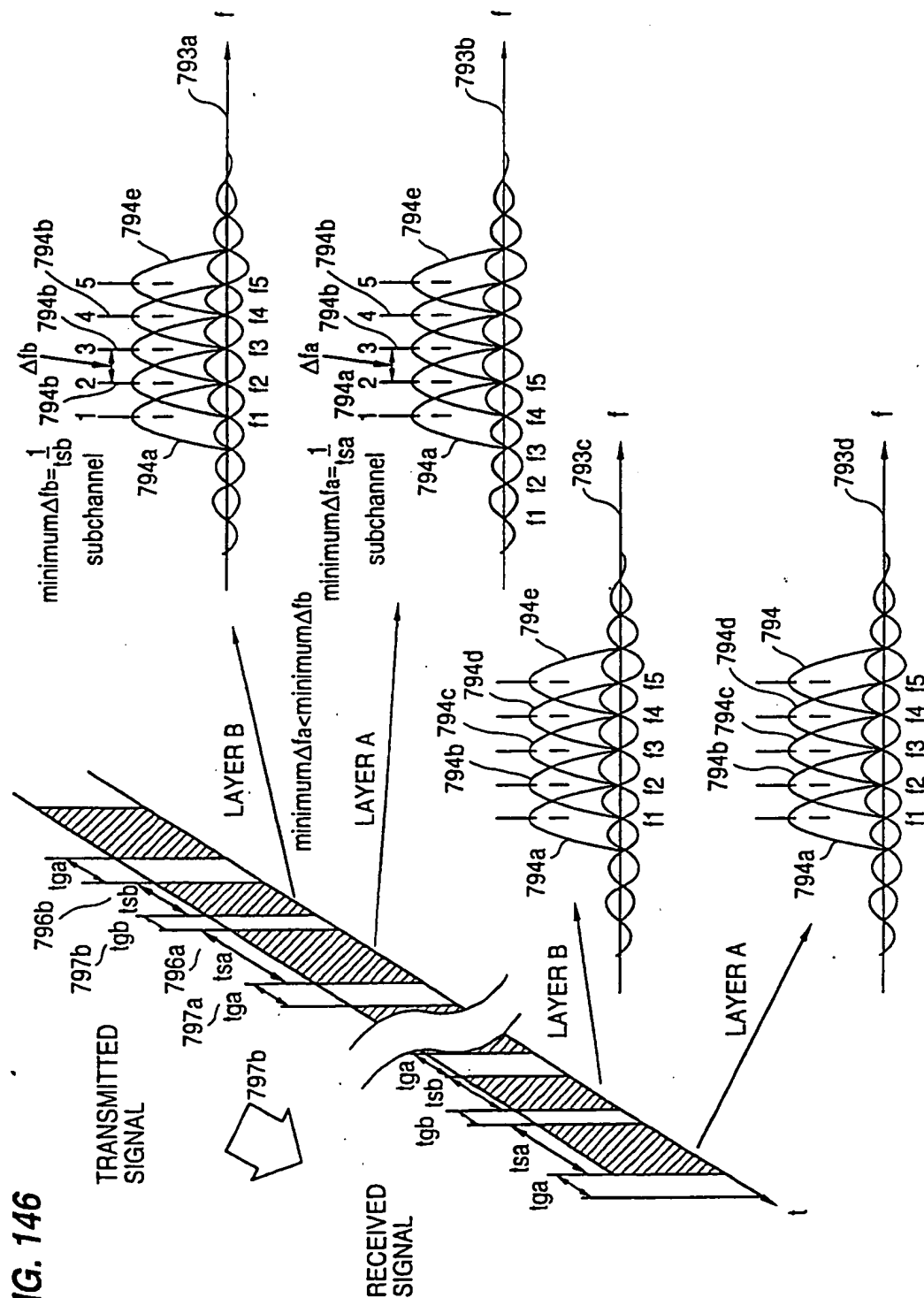


FIG. 147

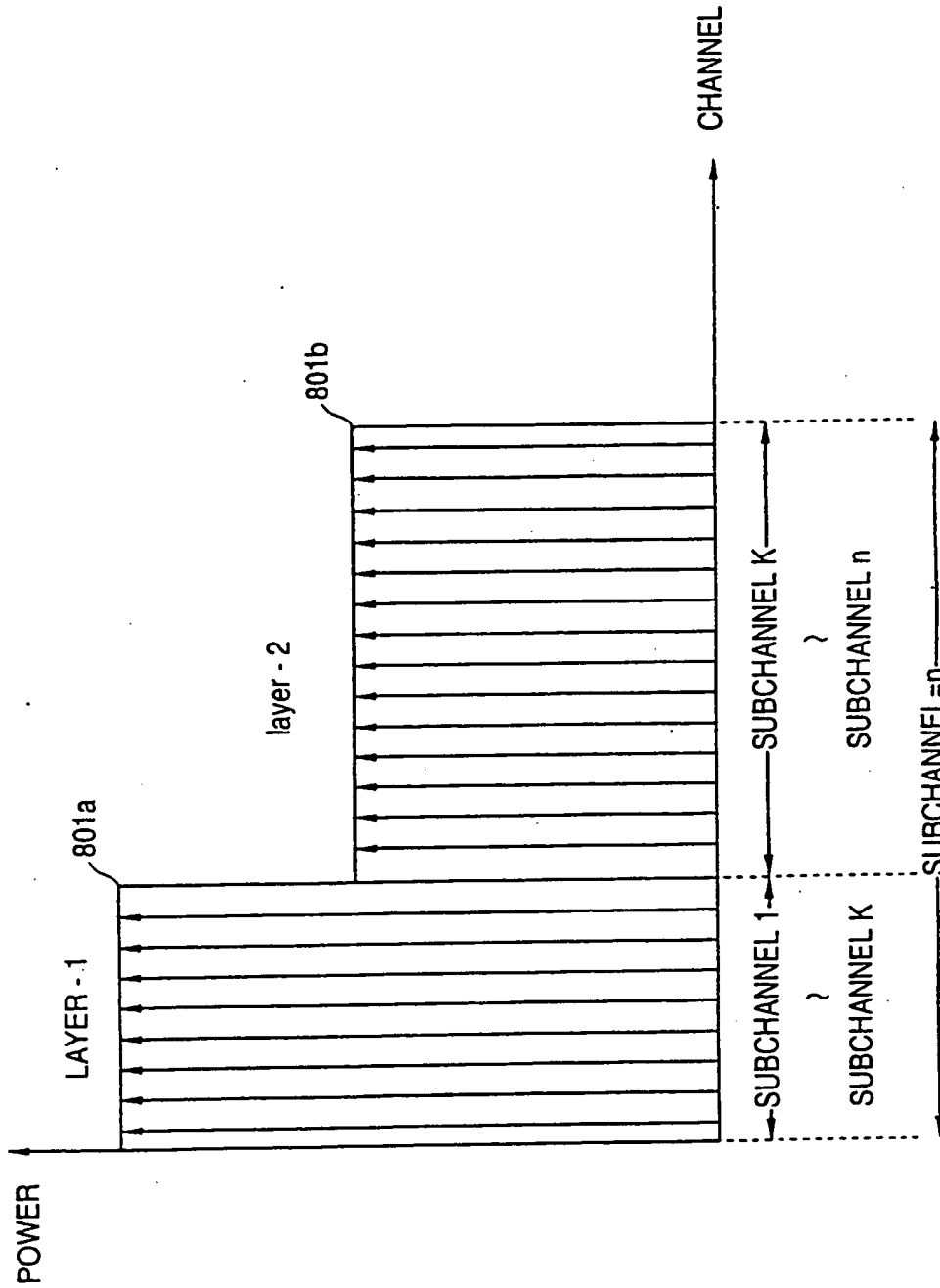
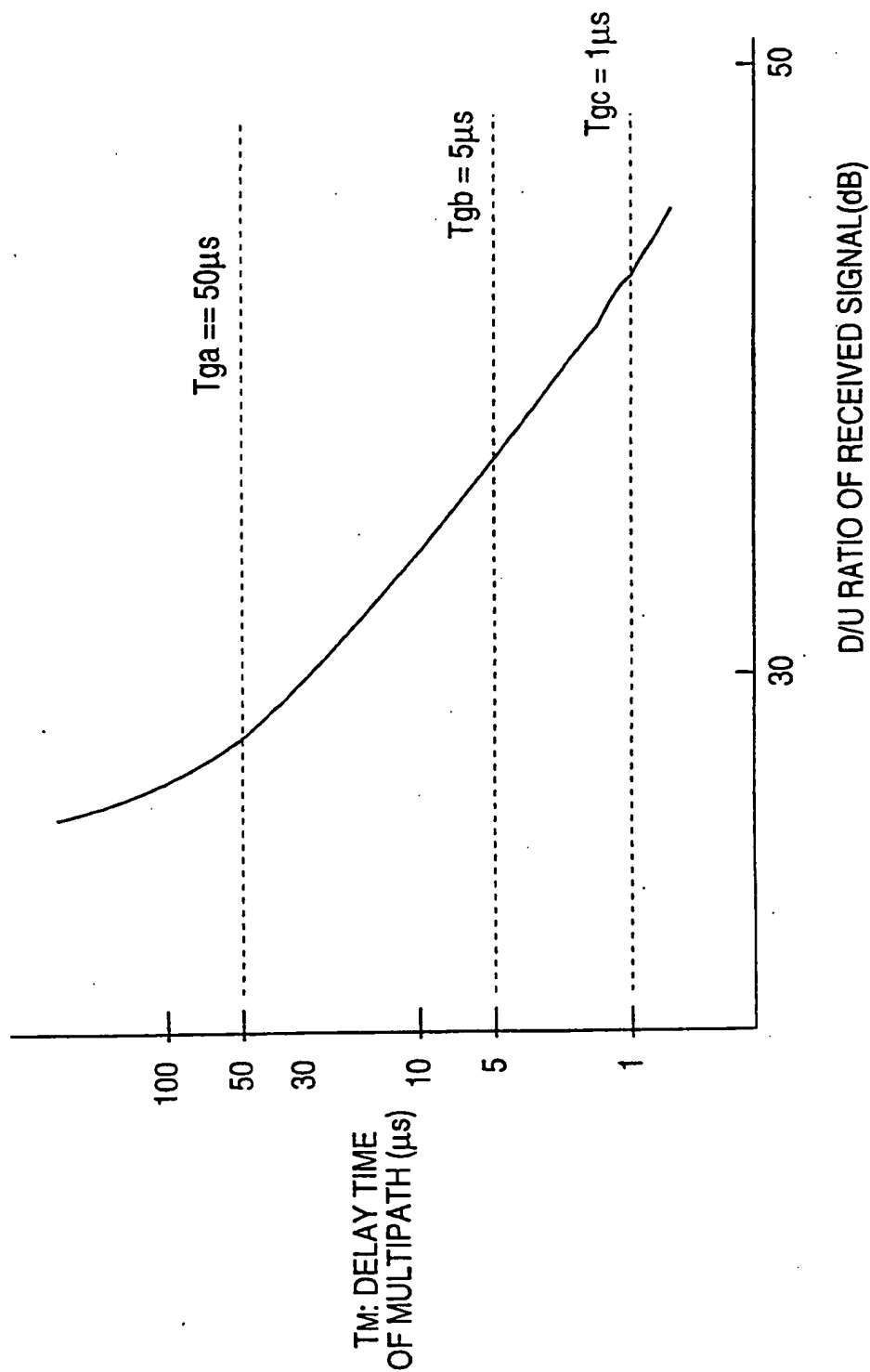


FIG. 148



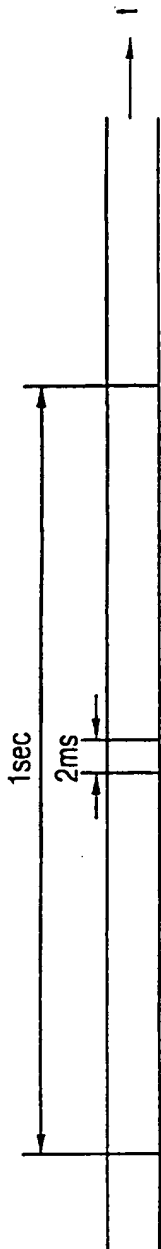


FIG. 149(a)

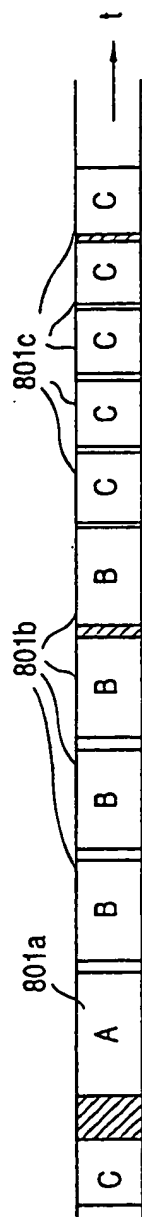


FIG. 149(b)

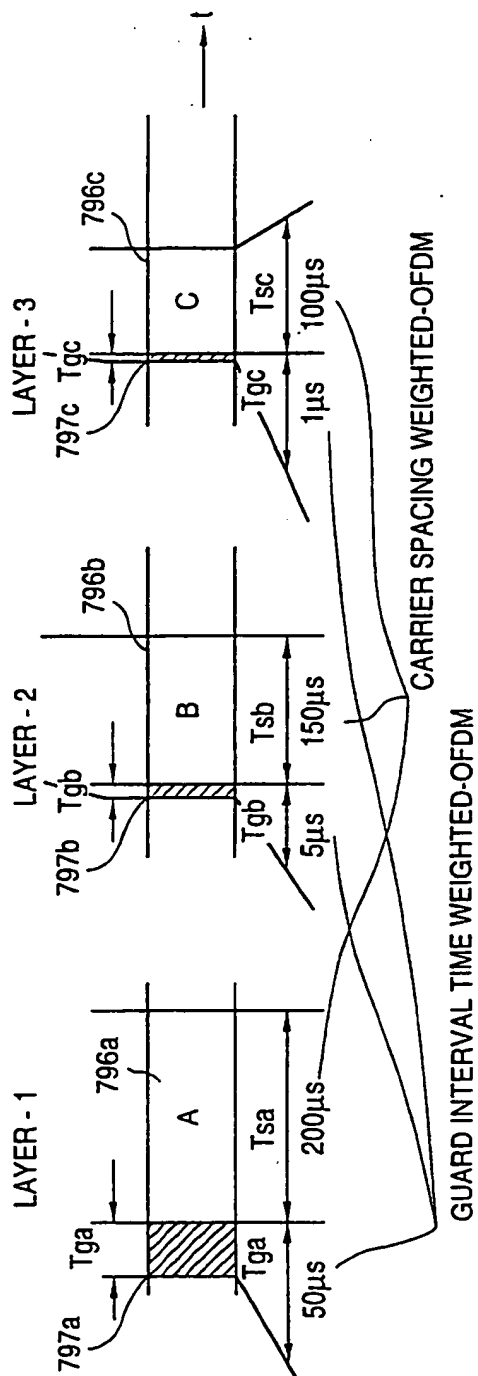


FIG. 149(c)

FIG. 150

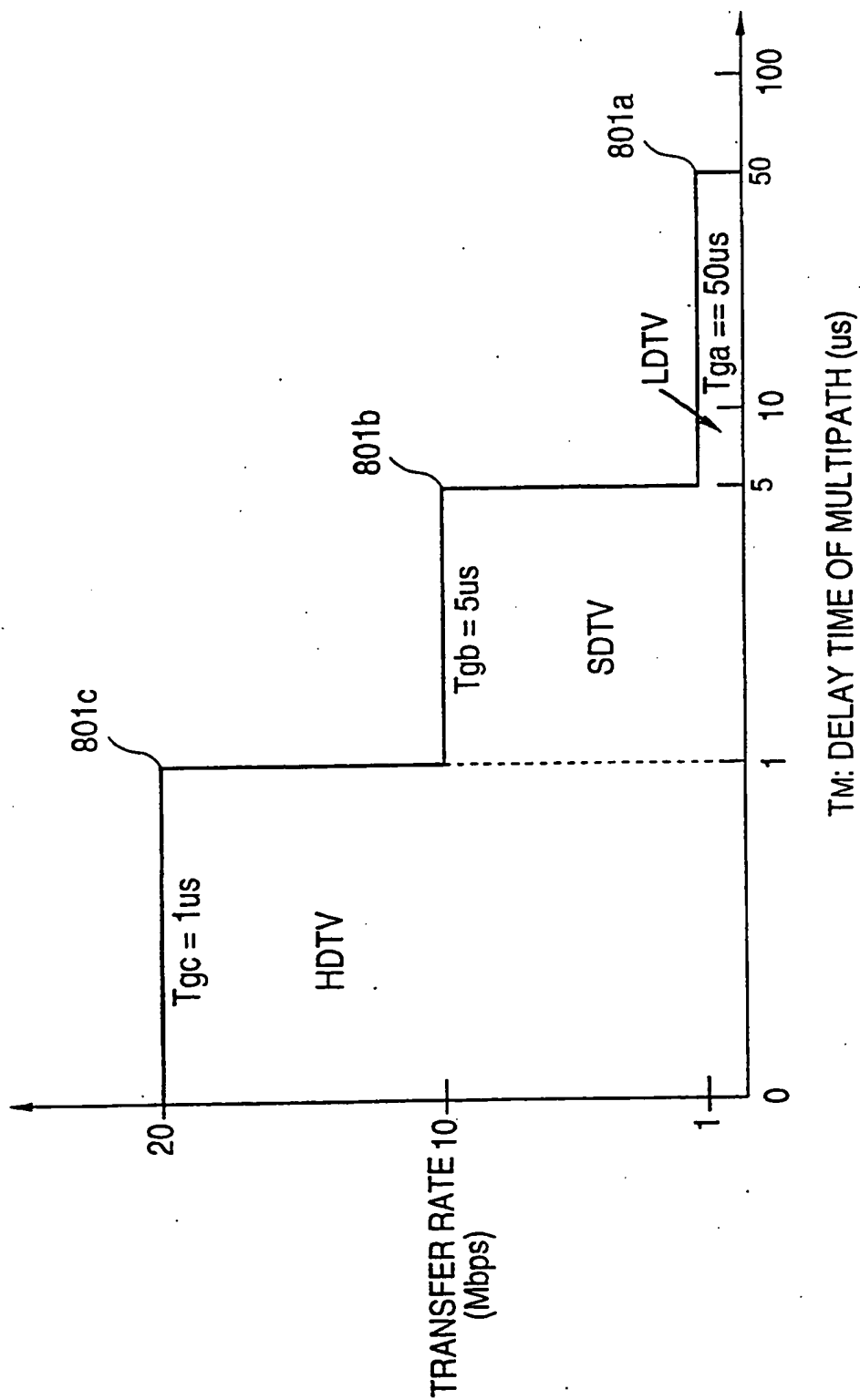


FIG. 151

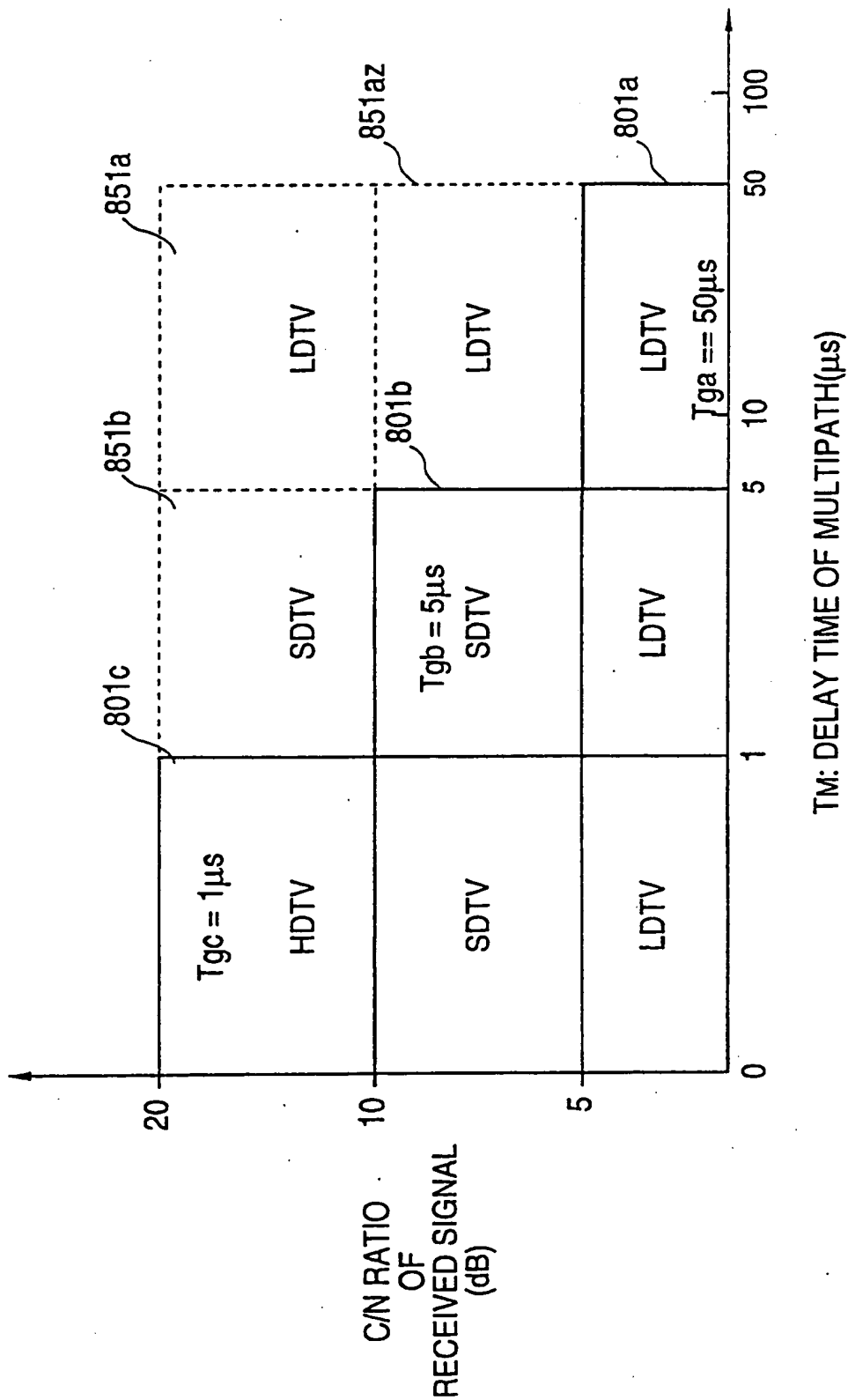


FIG. 152

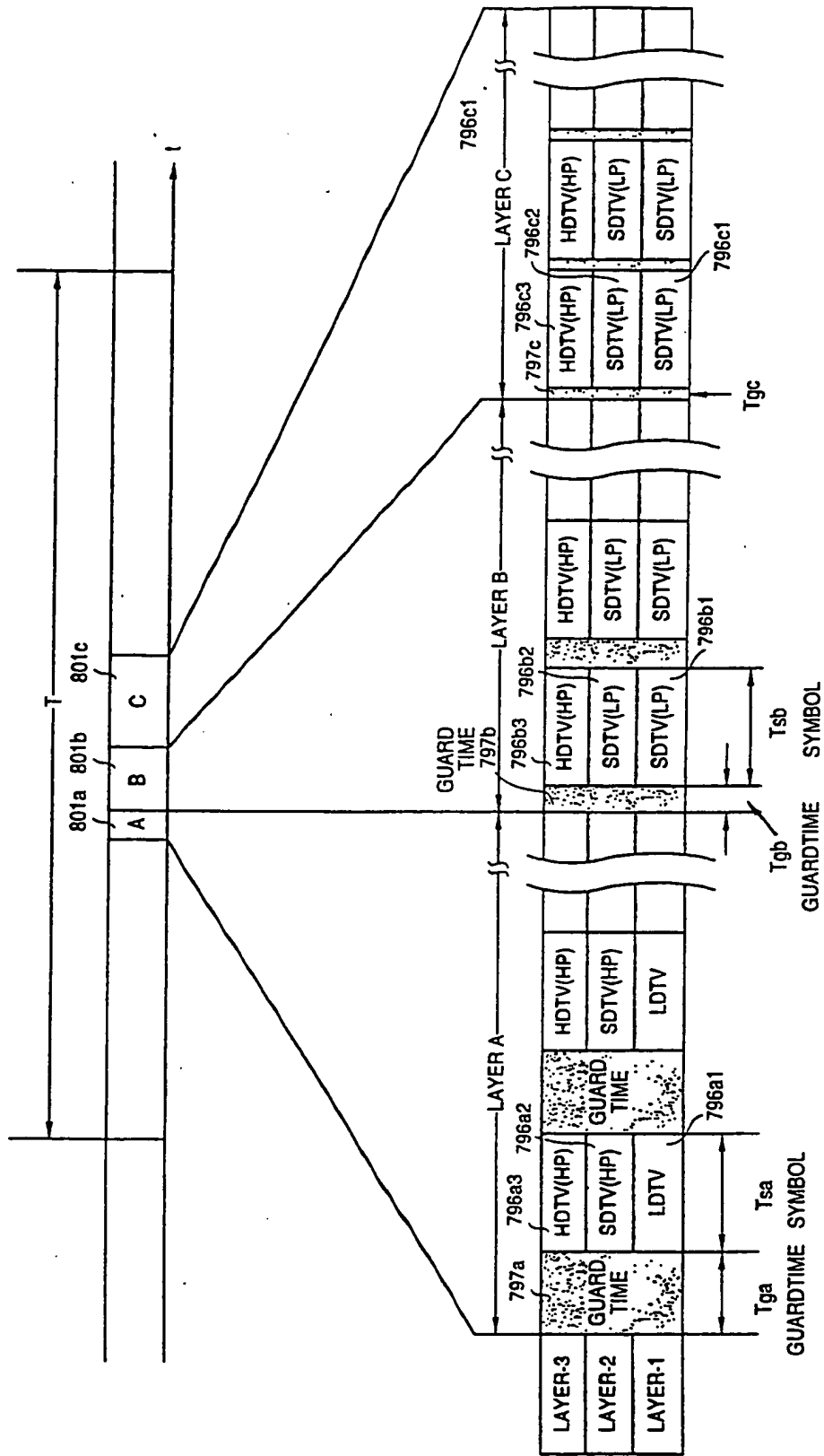
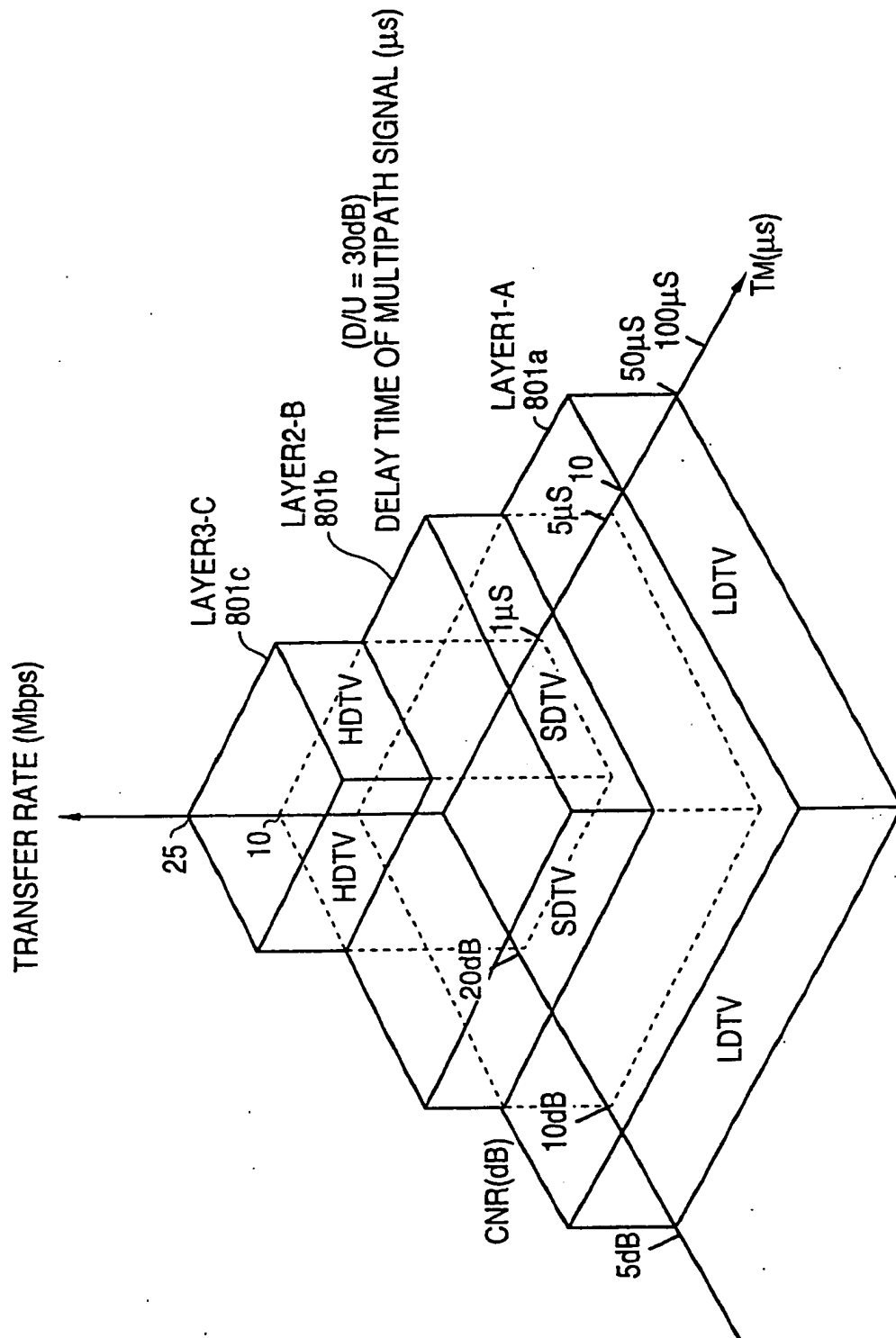


FIG. 153



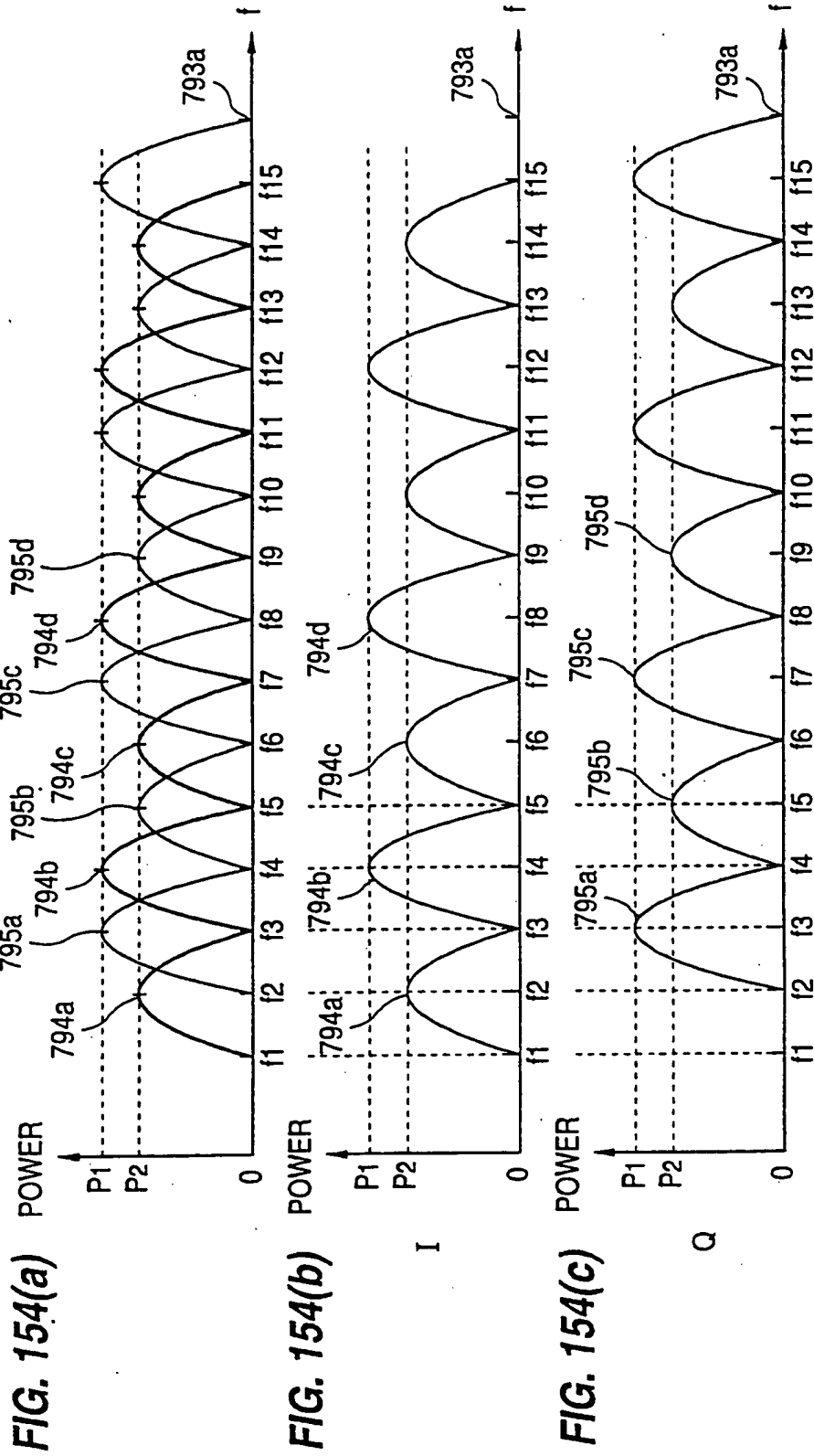


FIG. 155

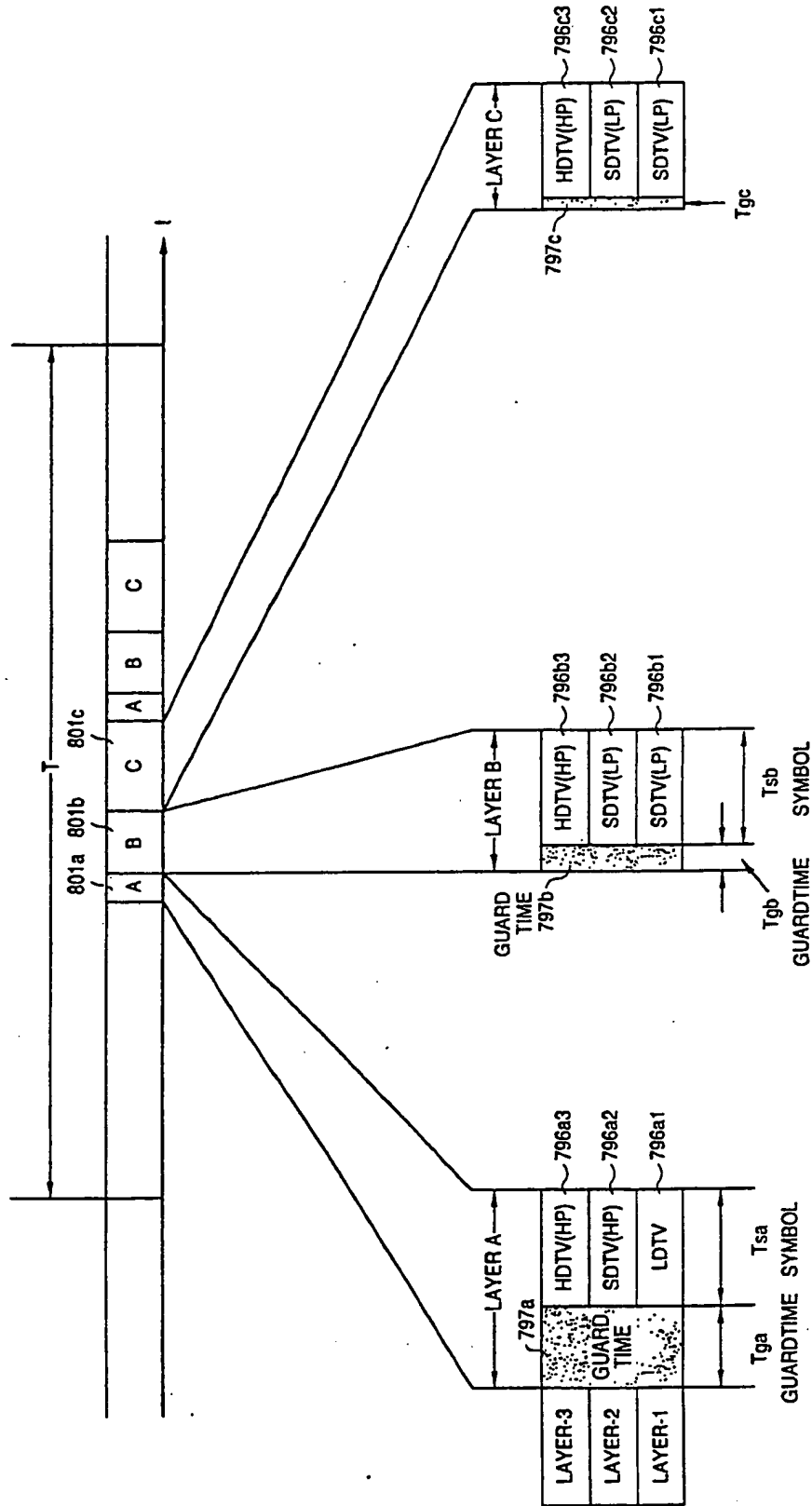


FIG. 156

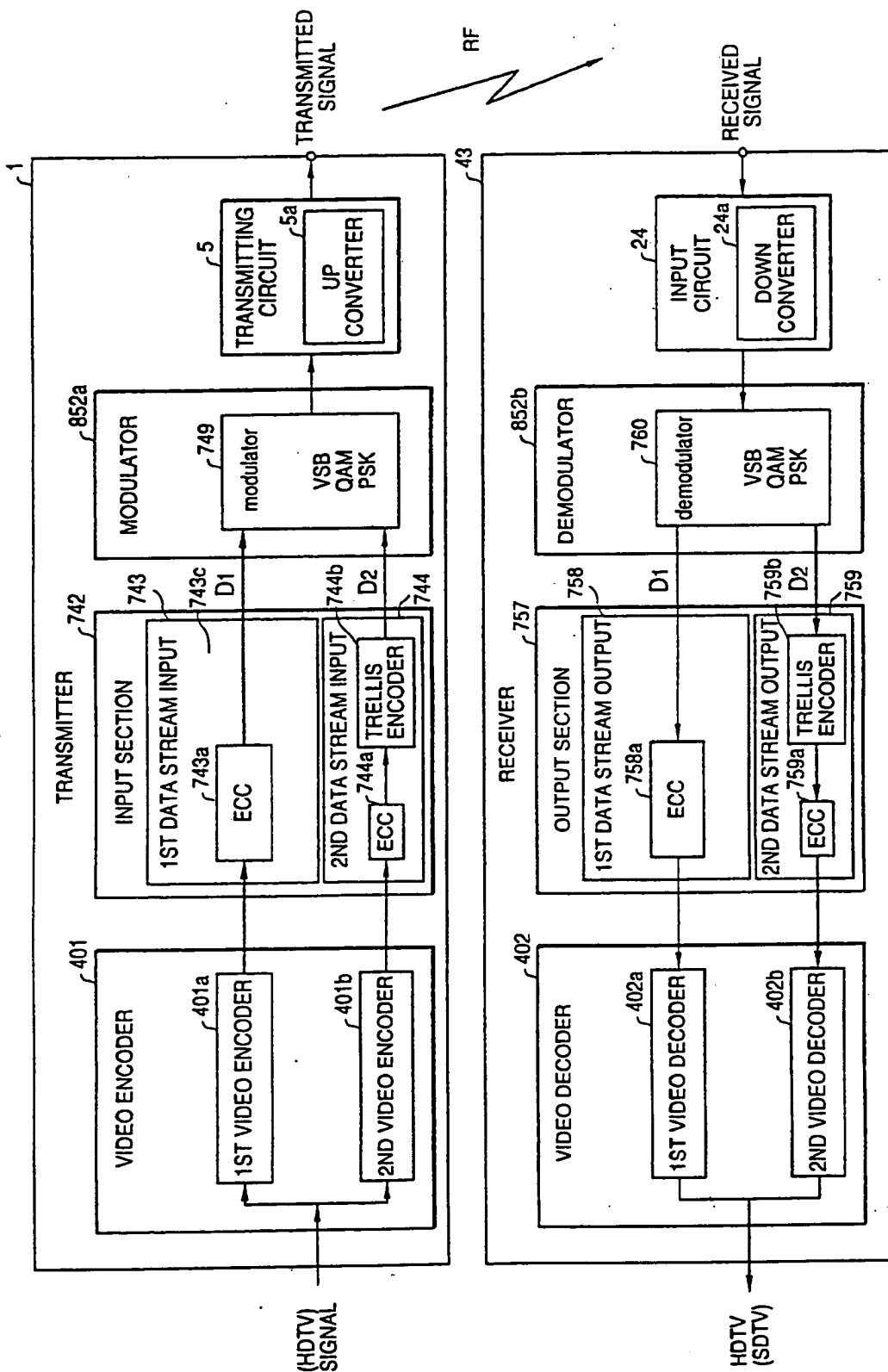


FIG. 157

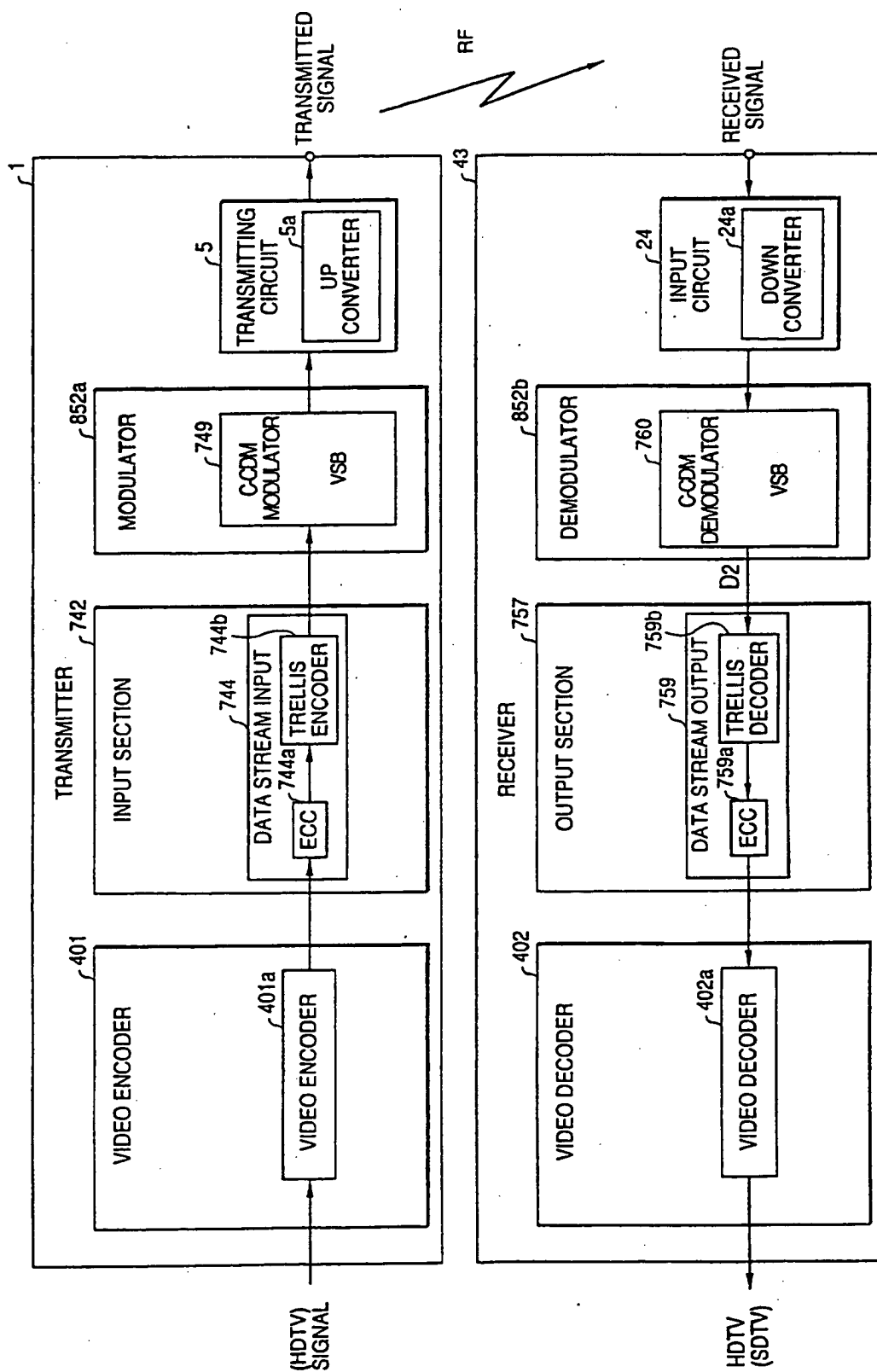
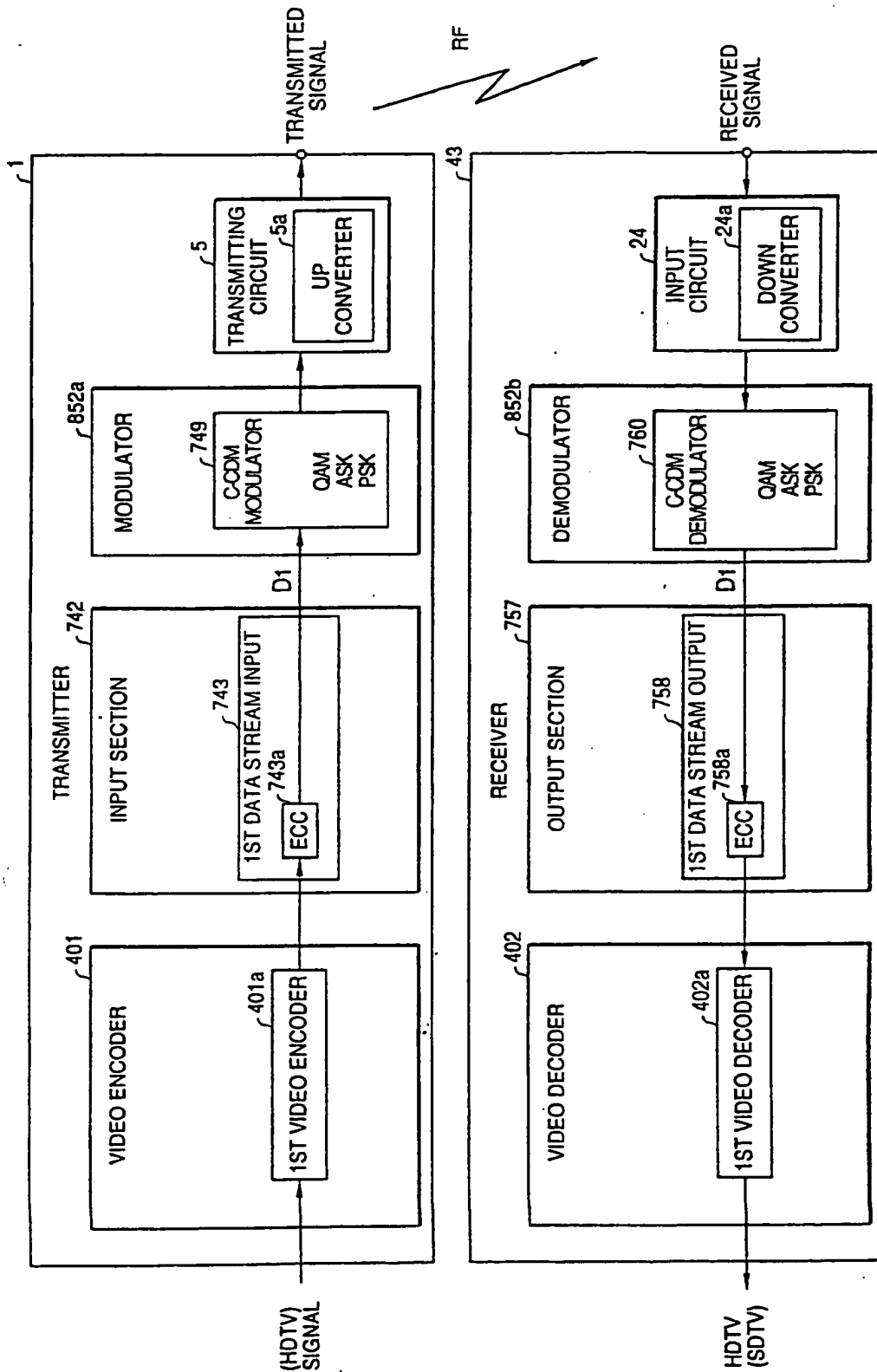


FIG. 158



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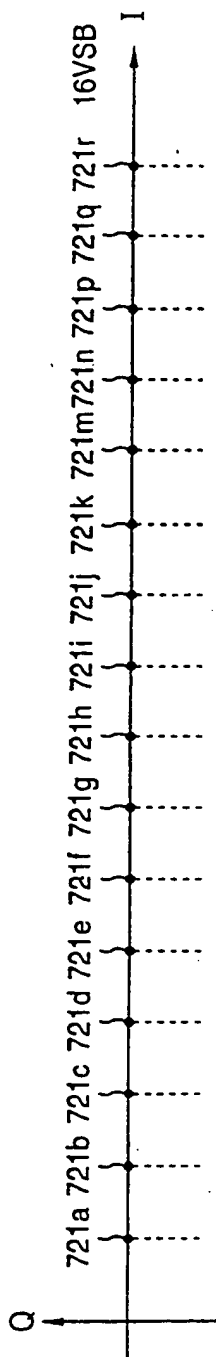


FIG. 159(a)

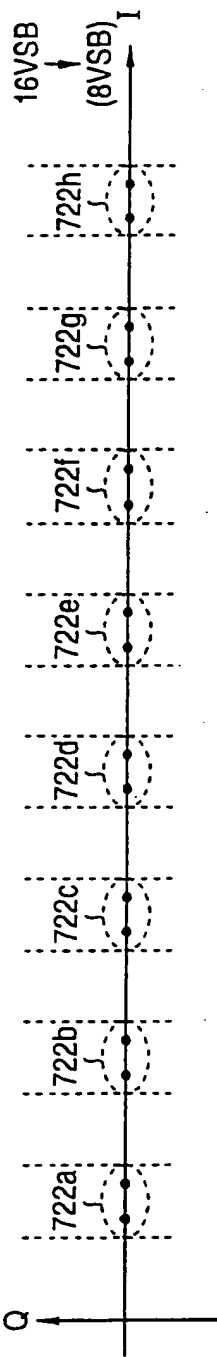


FIG. 159(b)

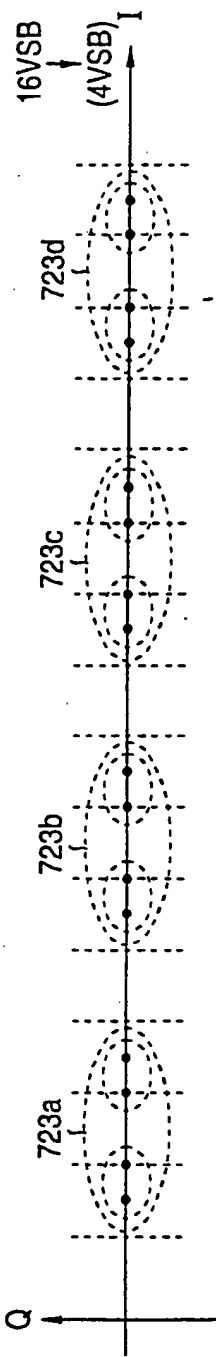


FIG. 159(c)

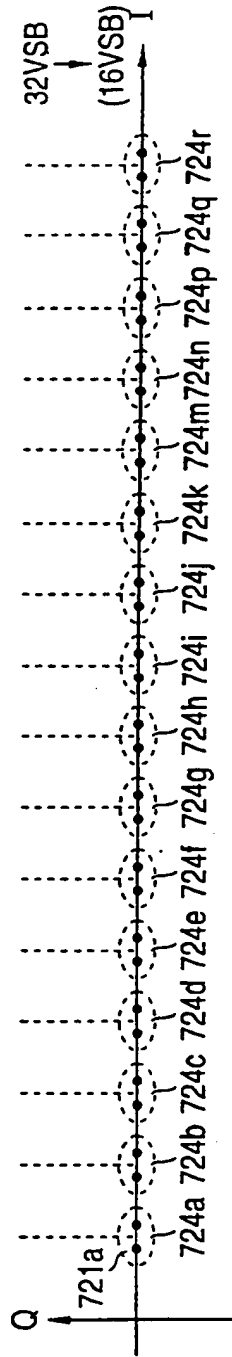


FIG. 159(d)

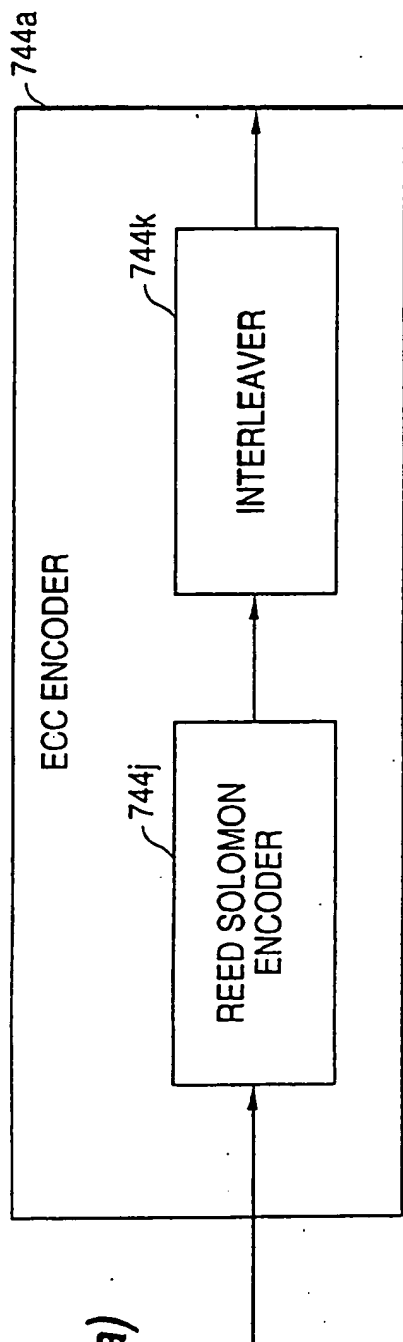


FIG. 160(a)

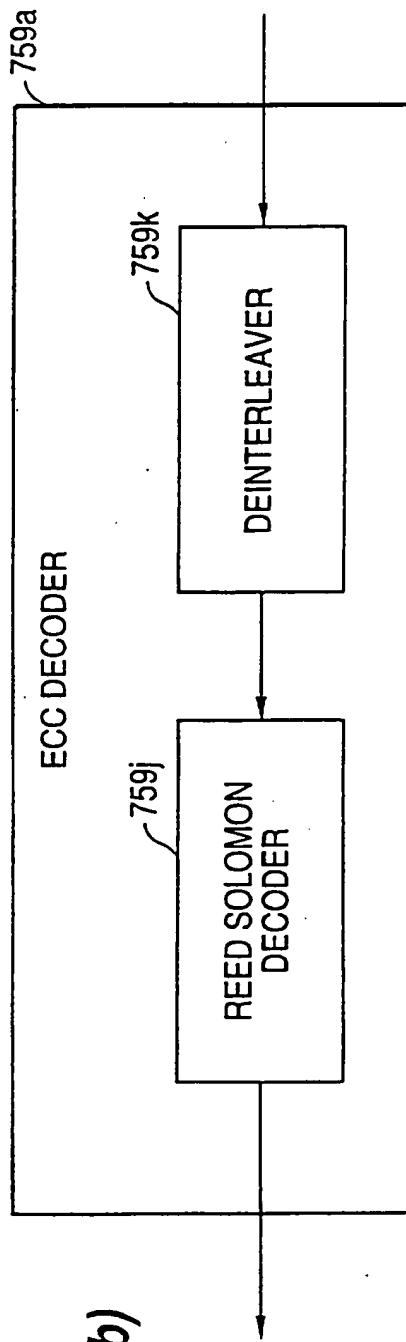


FIG. 160(b)

FIG. 161

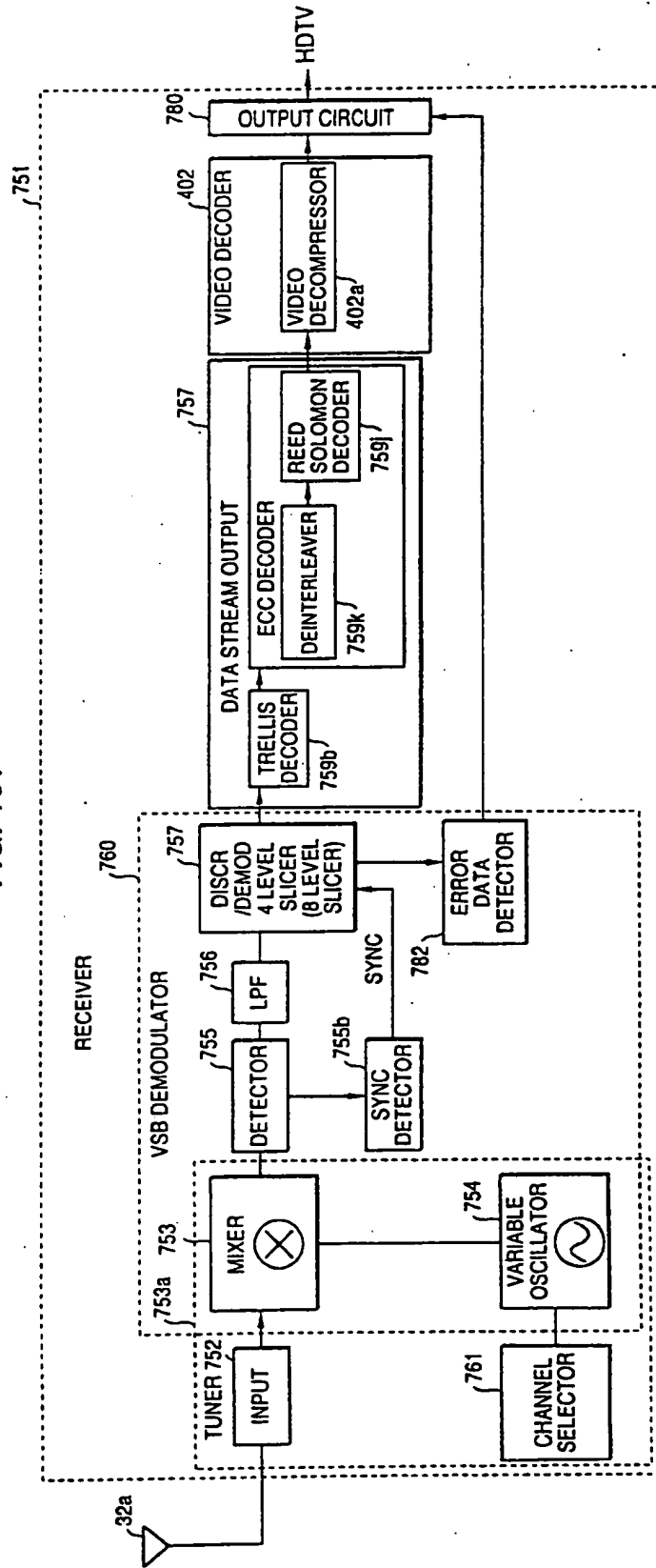


FIG. 162

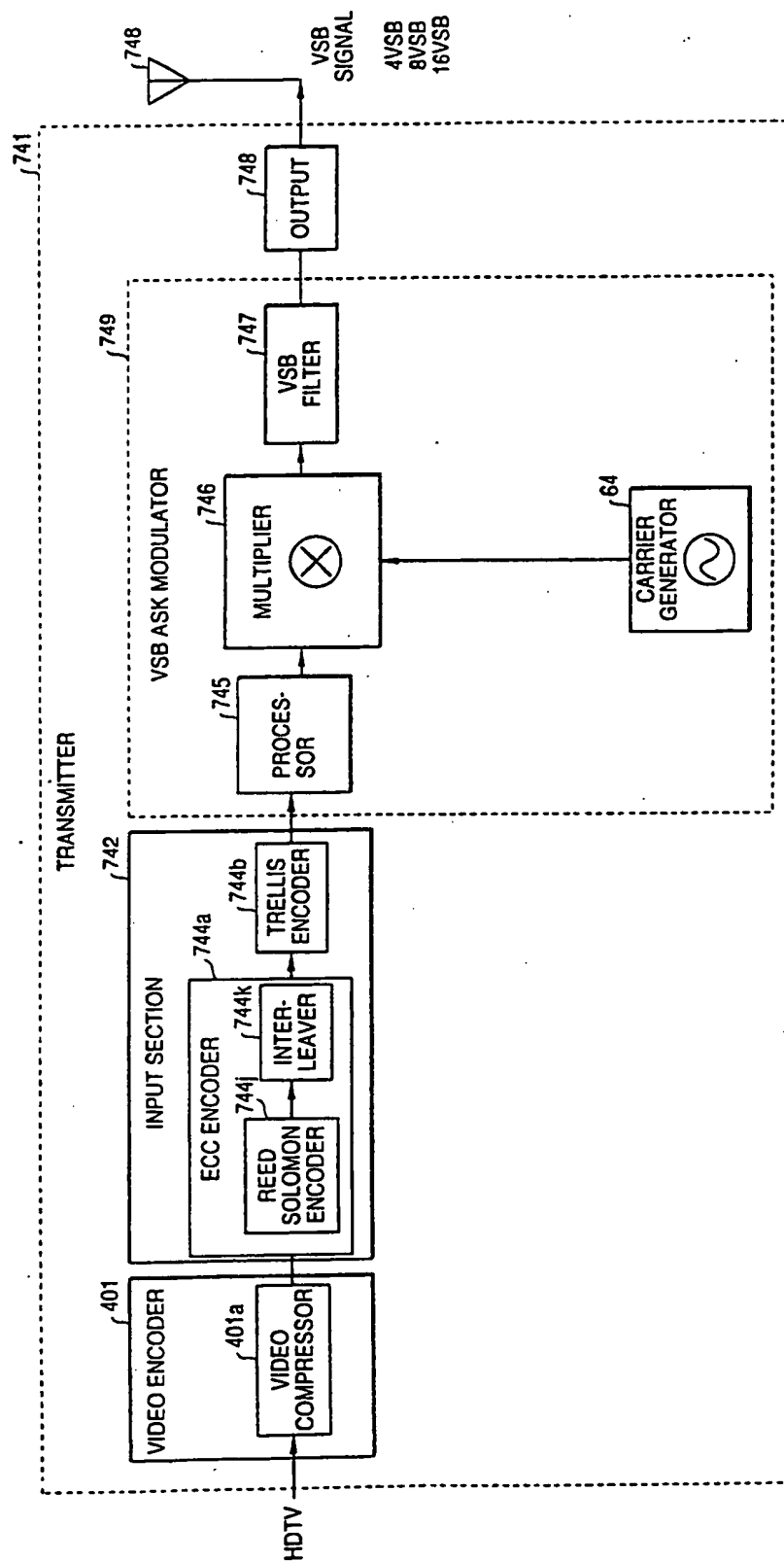
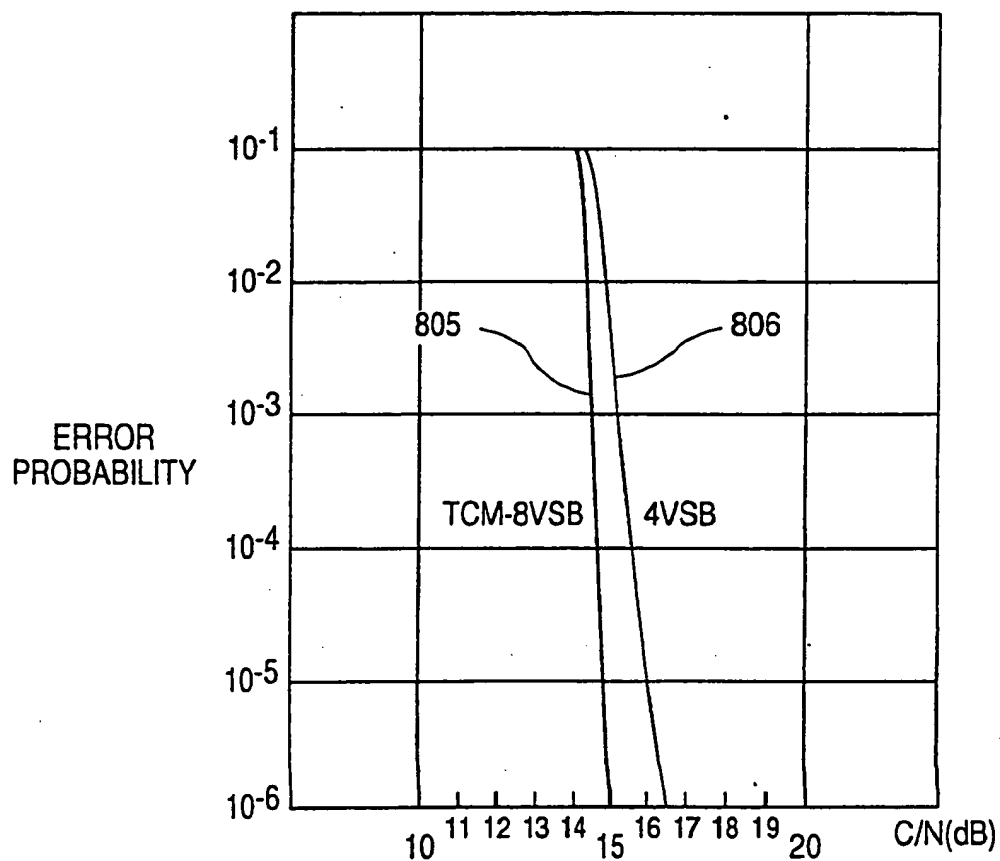


FIG. 163



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FIG. 164

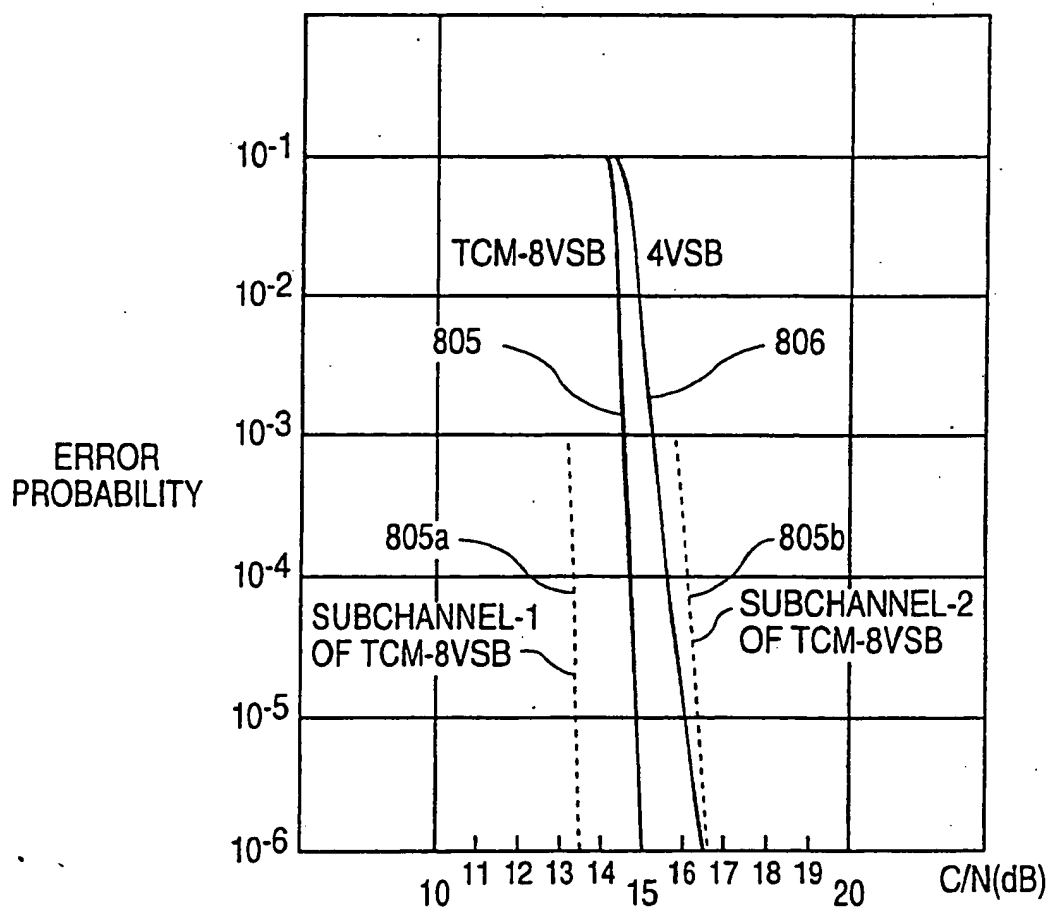


FIG. 165(a)

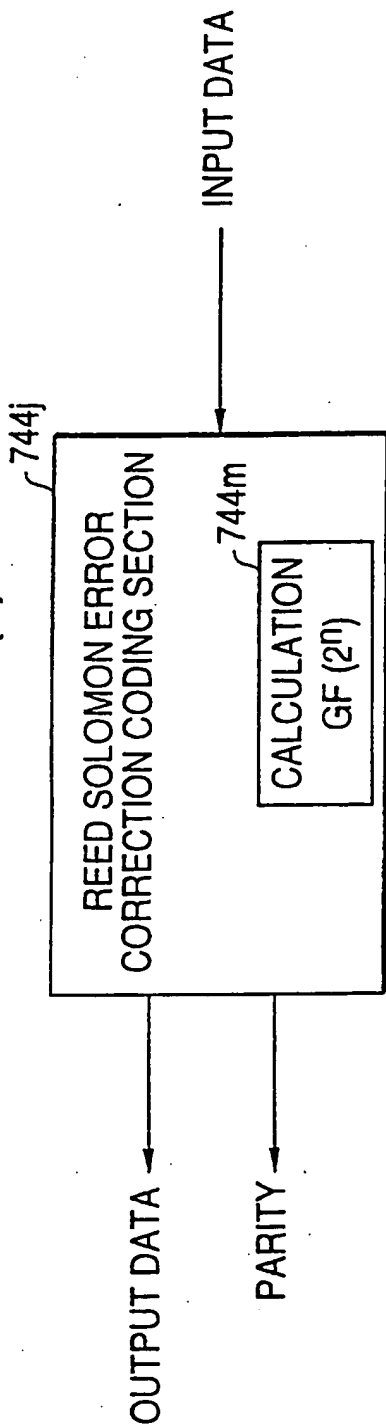


FIG. 165(b)

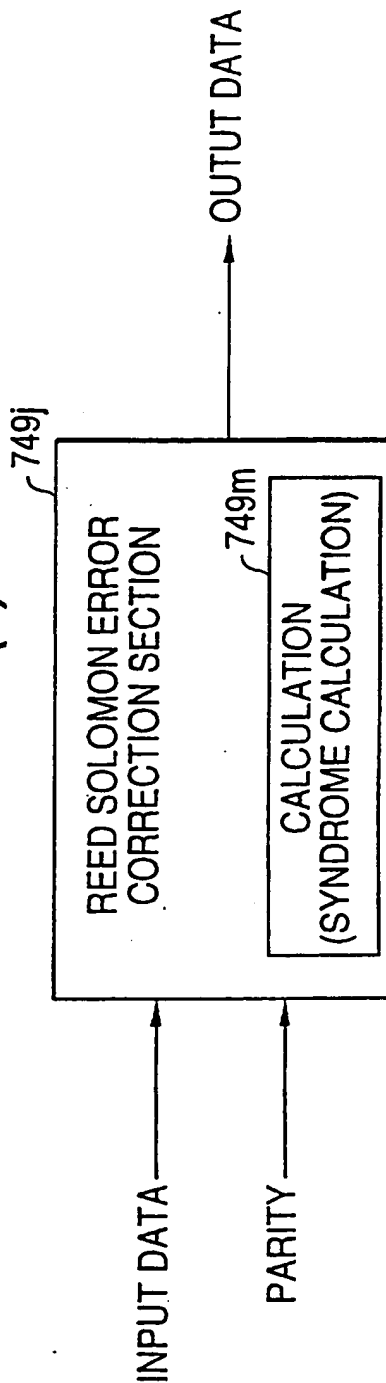


FIG. 166

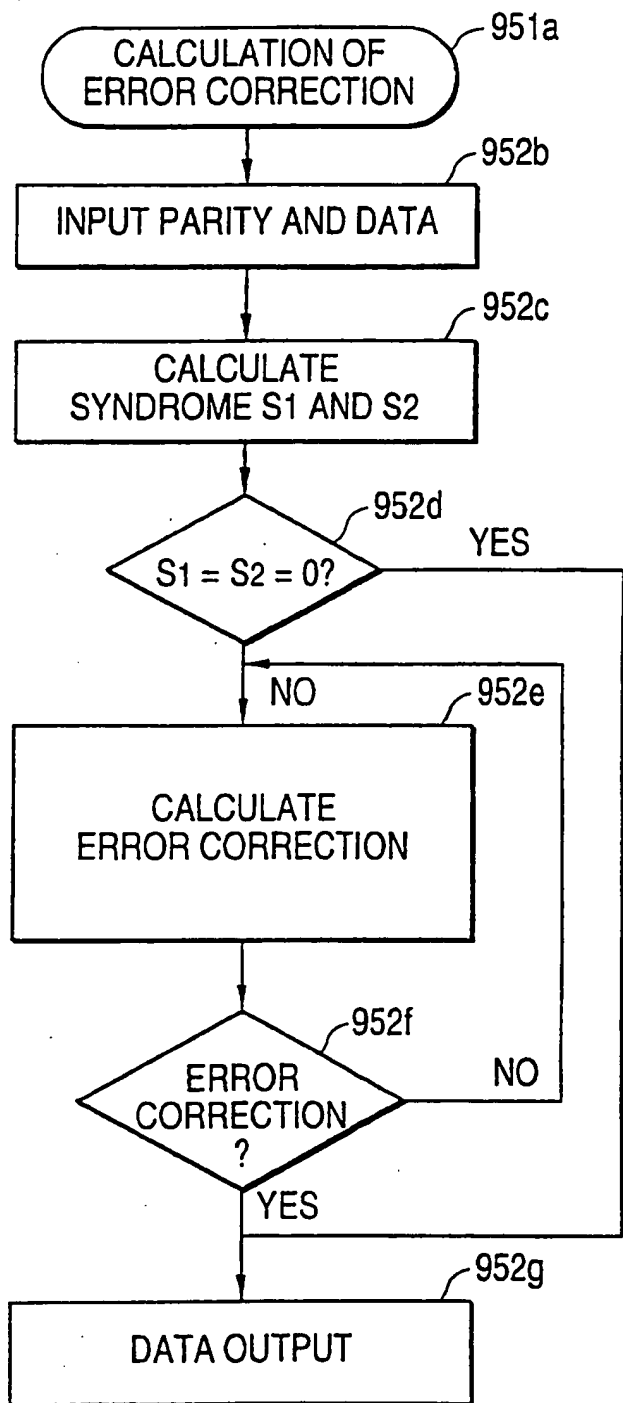


FIG. 167

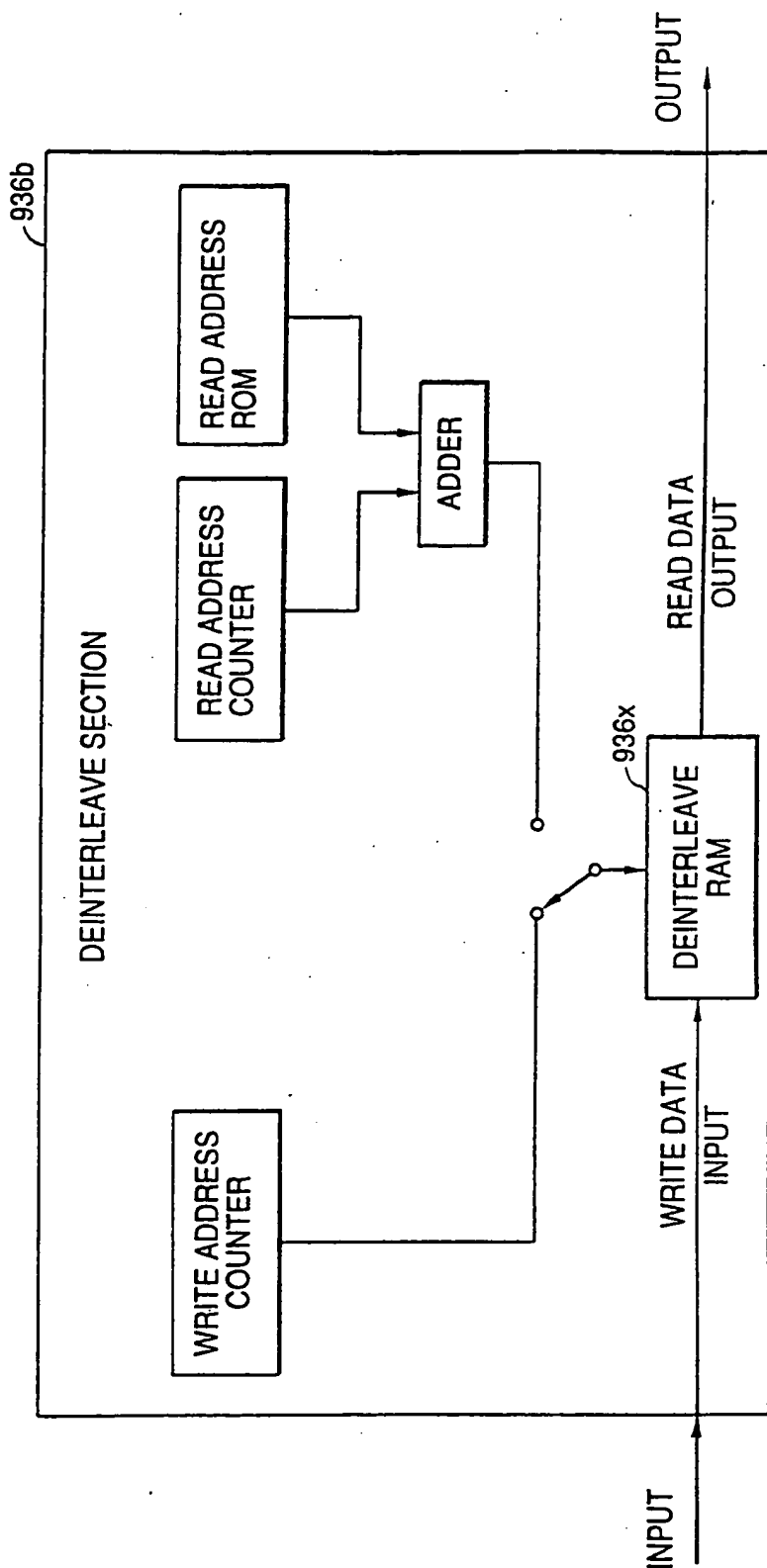


FIG. 168(a)

INTERLEAVE TABLE

	1	2	3	4	5	6	7
	DATA						C2 PARITY
1	A 1	A 2	A 3	A 4	A 5	A 6	PARITY
2	B 1	B 2	B 3	B 4			
3	C 1						
4	D 1						
5	E 1						
6	F 1						
C1 PARITY	PARITY	PARITY	PARITY	PARITY	PARITY	PARITY	PARITY

FIG. 168(b)

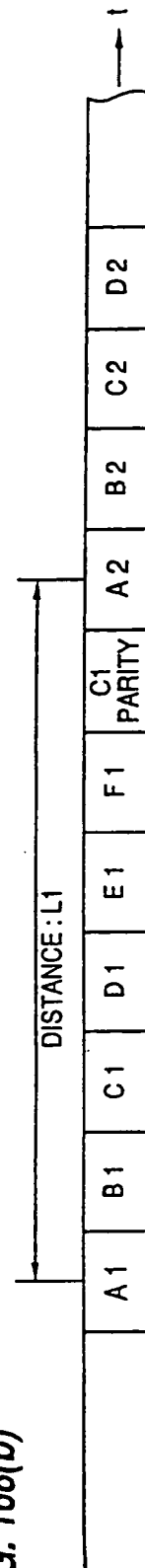


FIG. 169

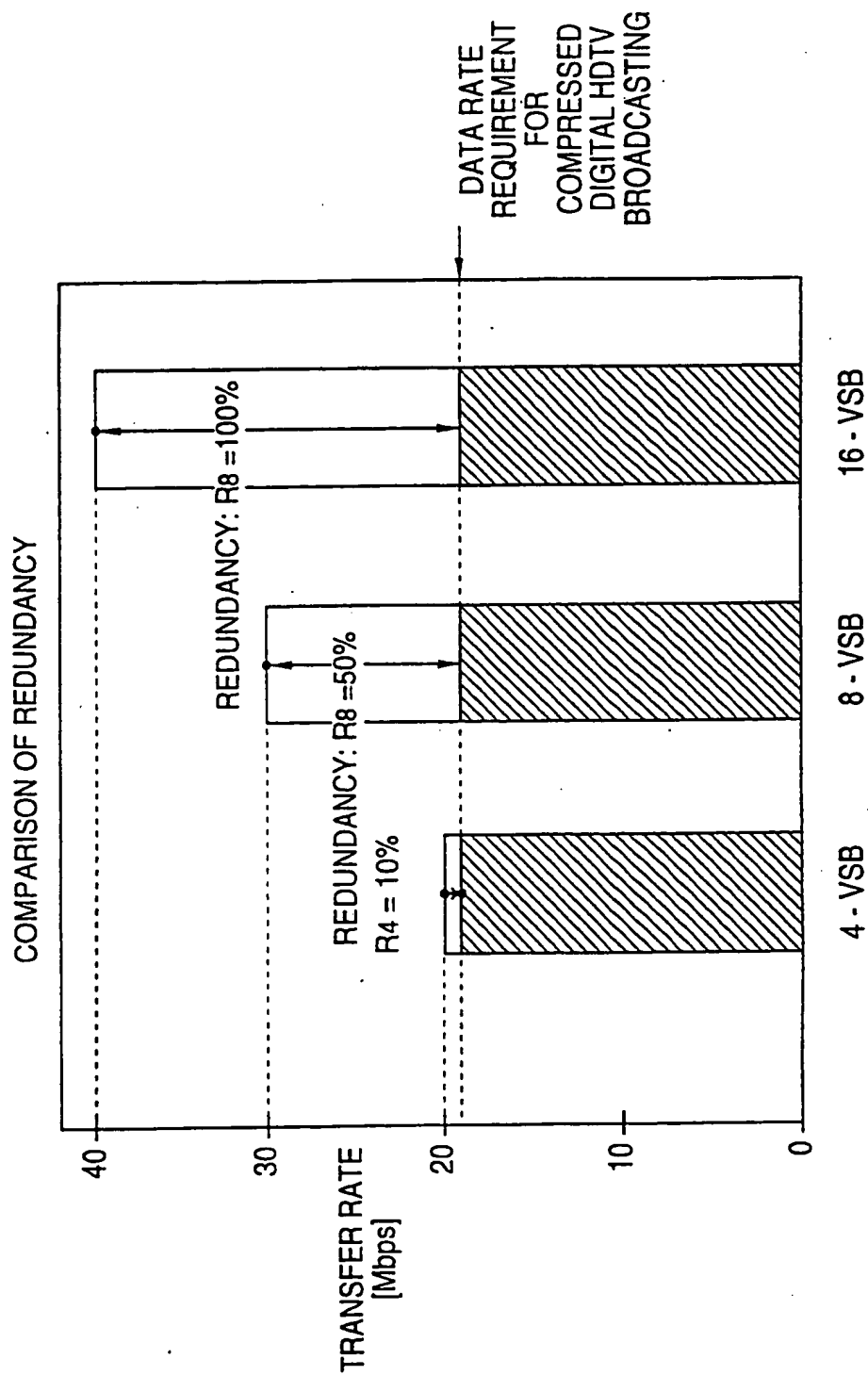


FIG. 170

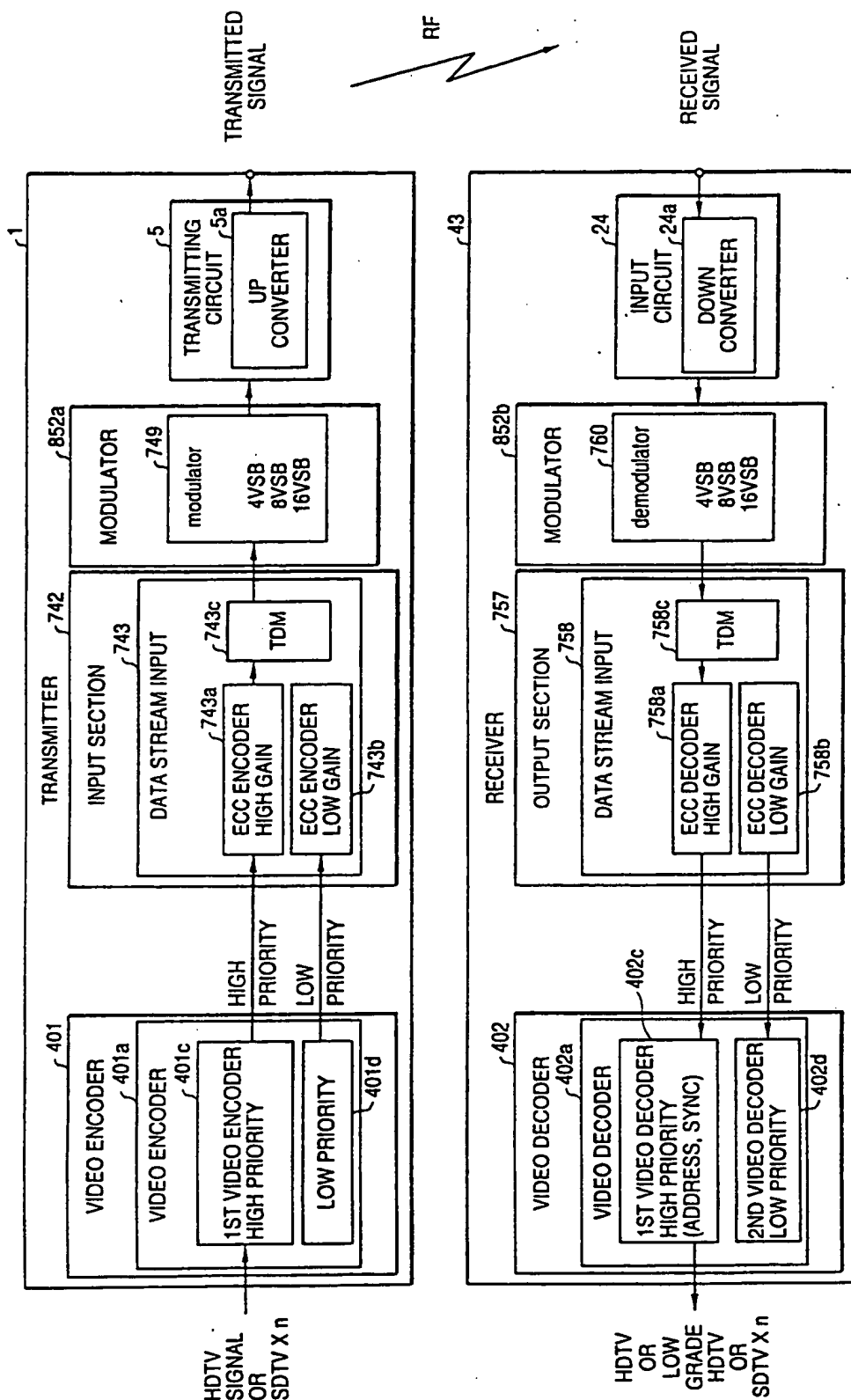


FIG. 171

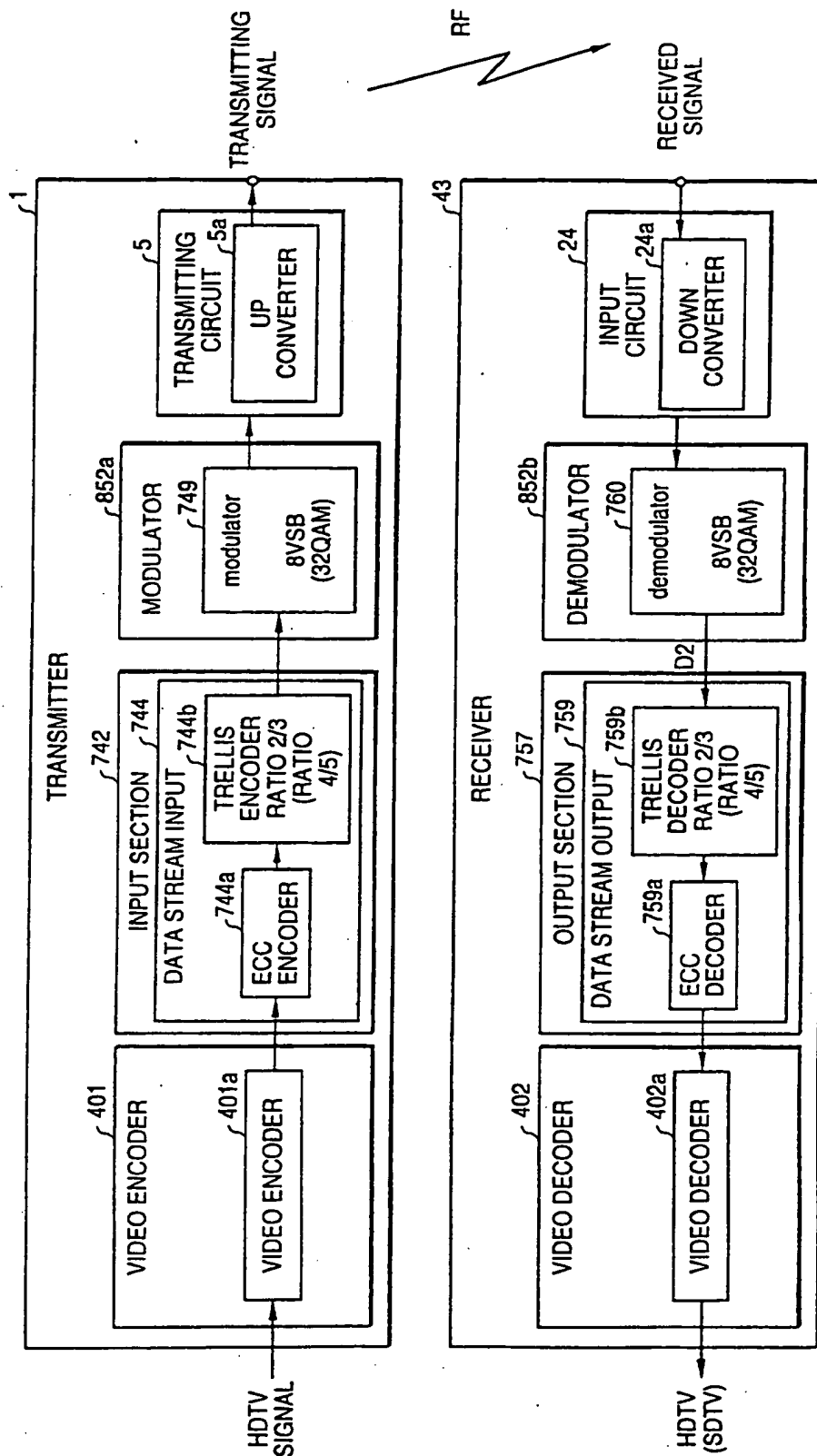
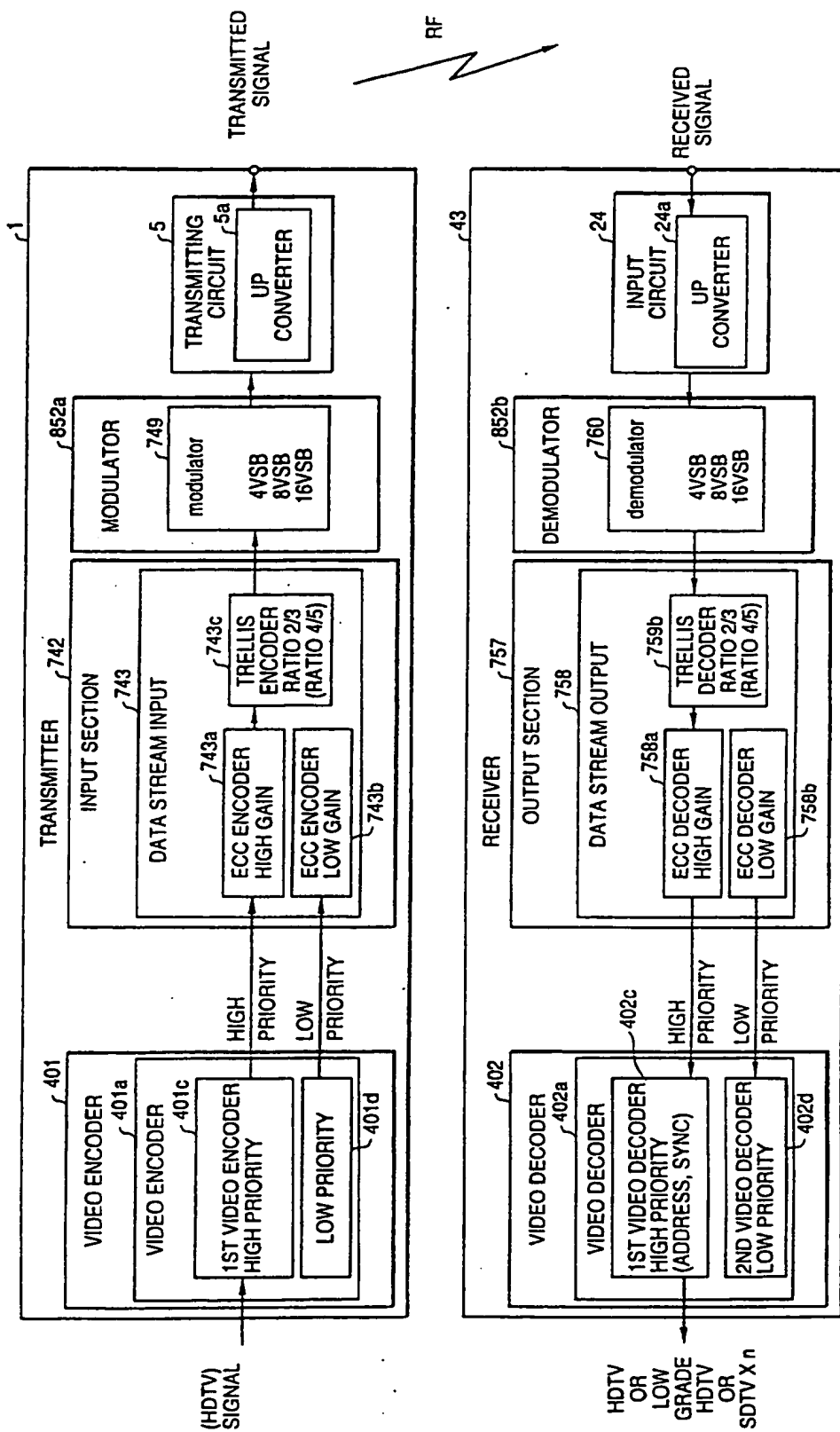


FIG. 172



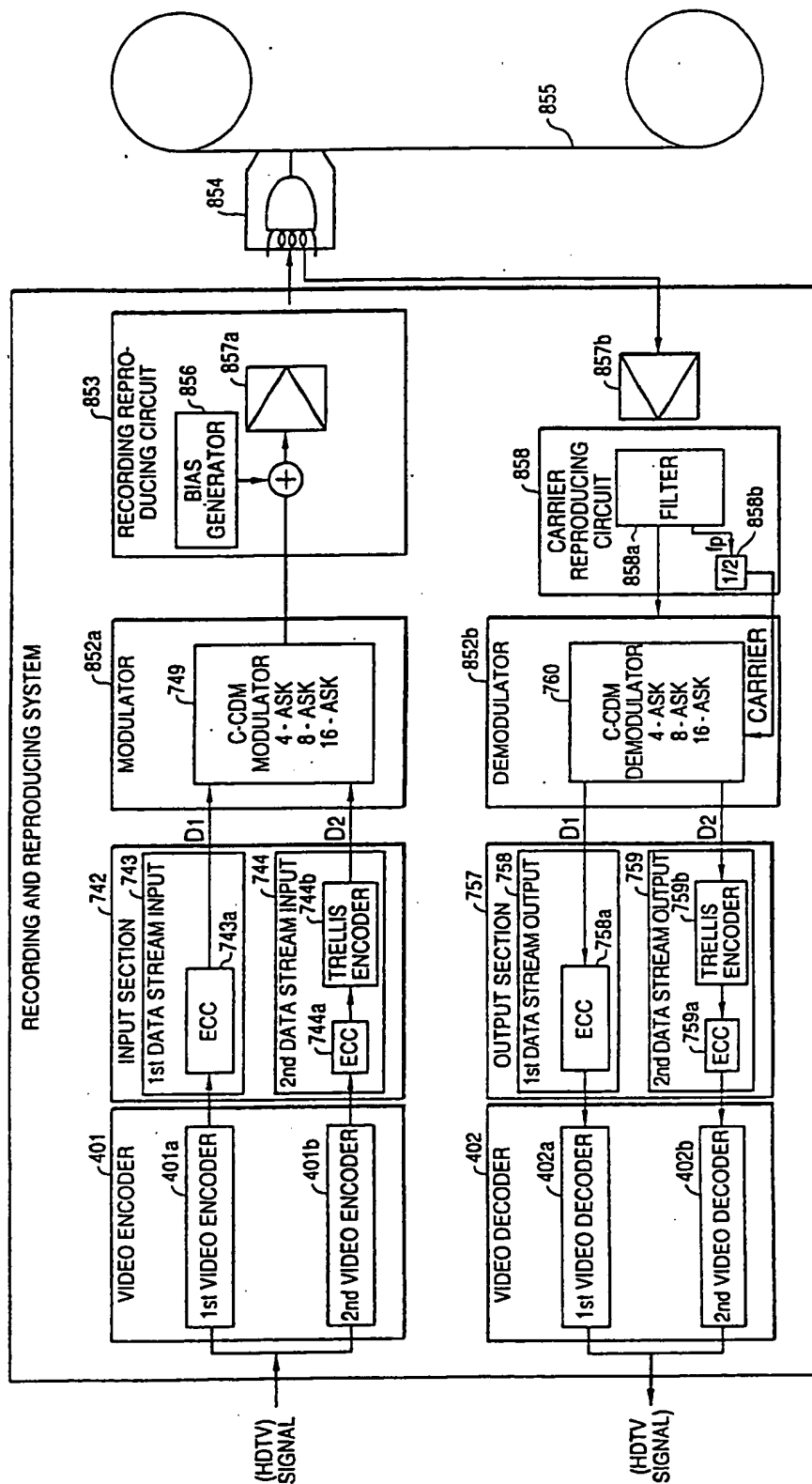


FIG. 174

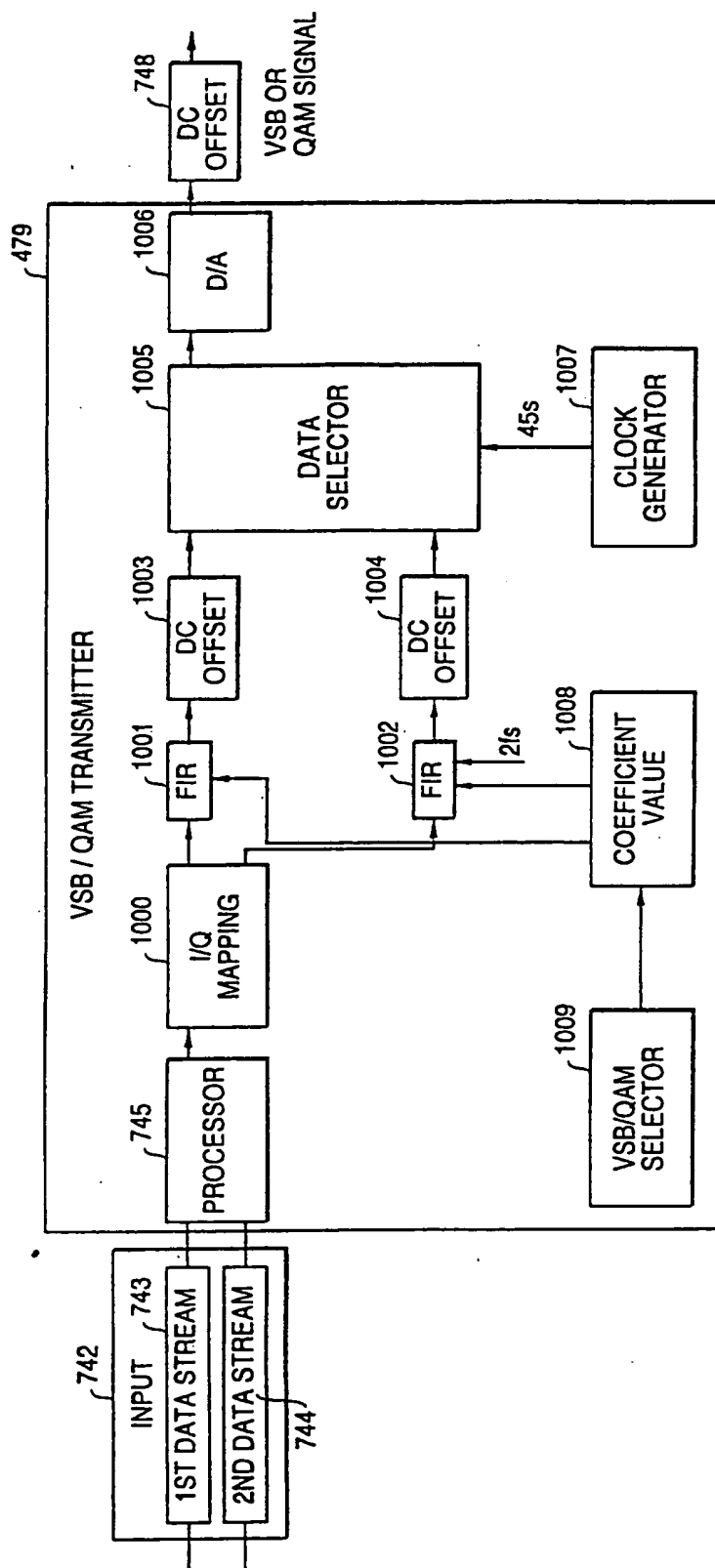


FIG. 175

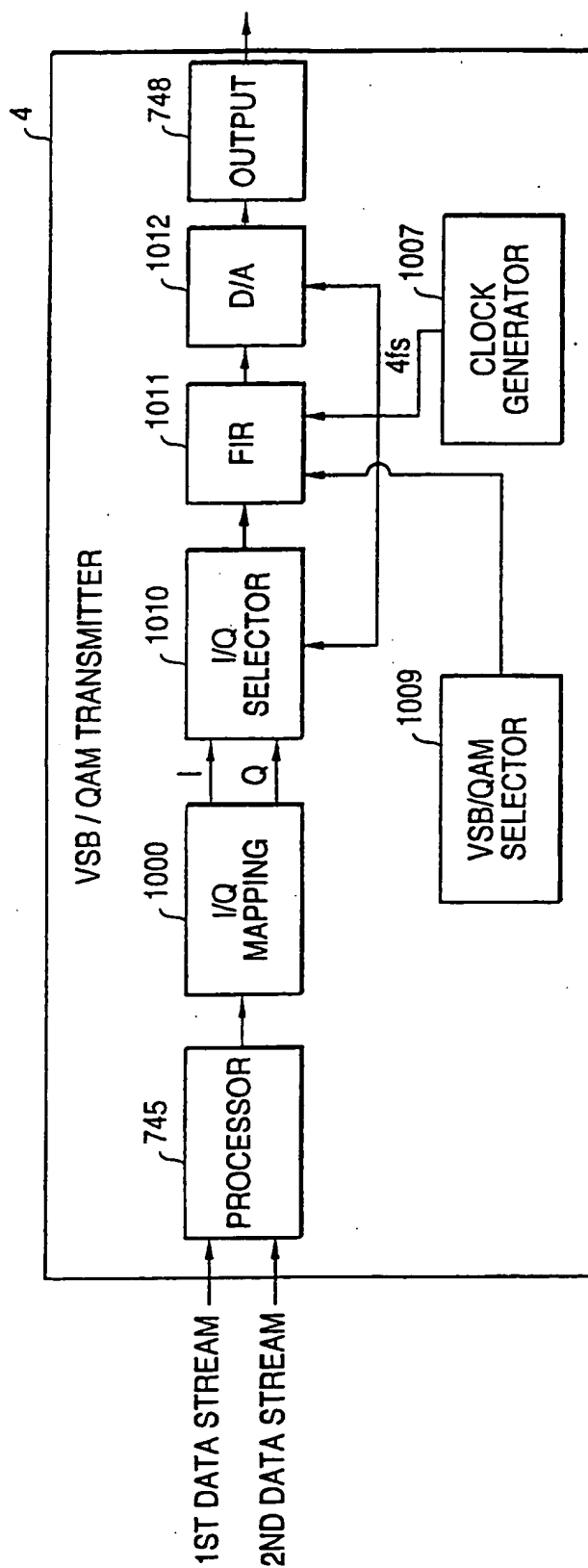


FIG. 176

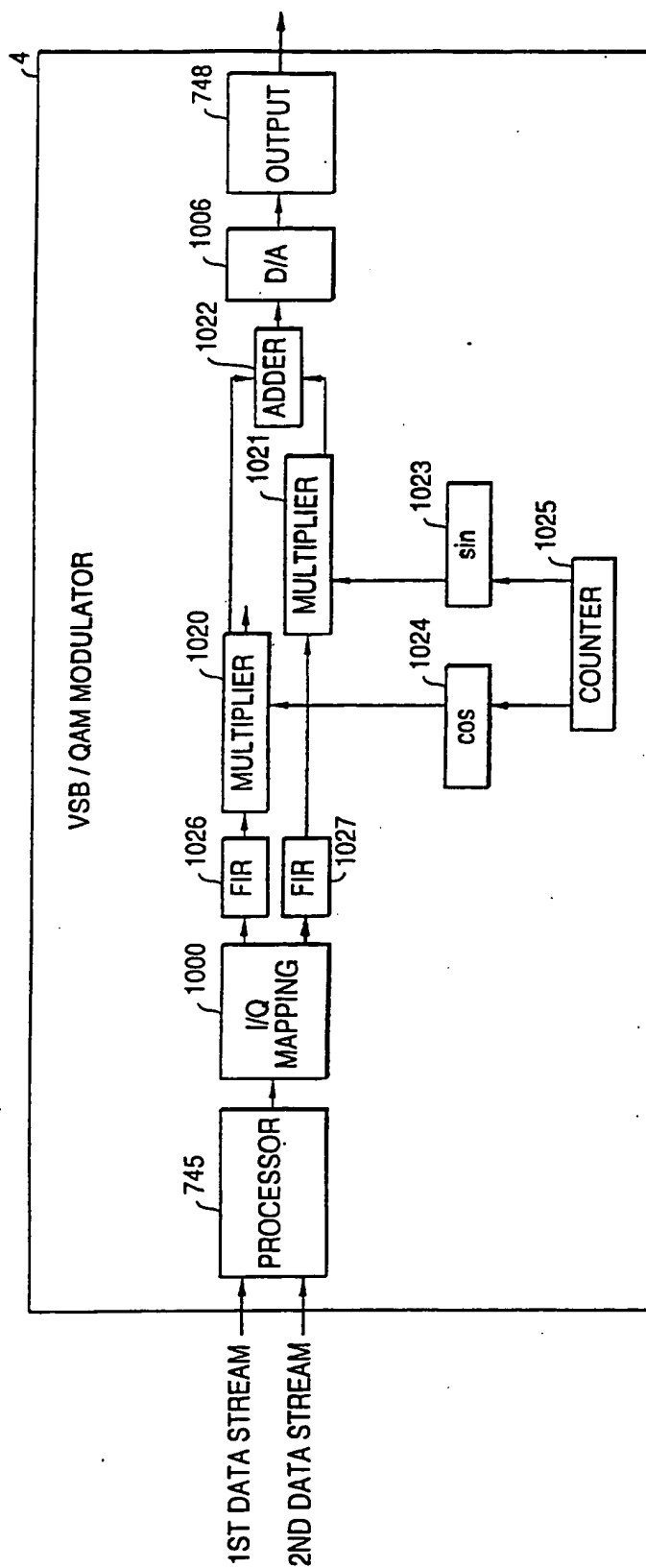


FIG. 177

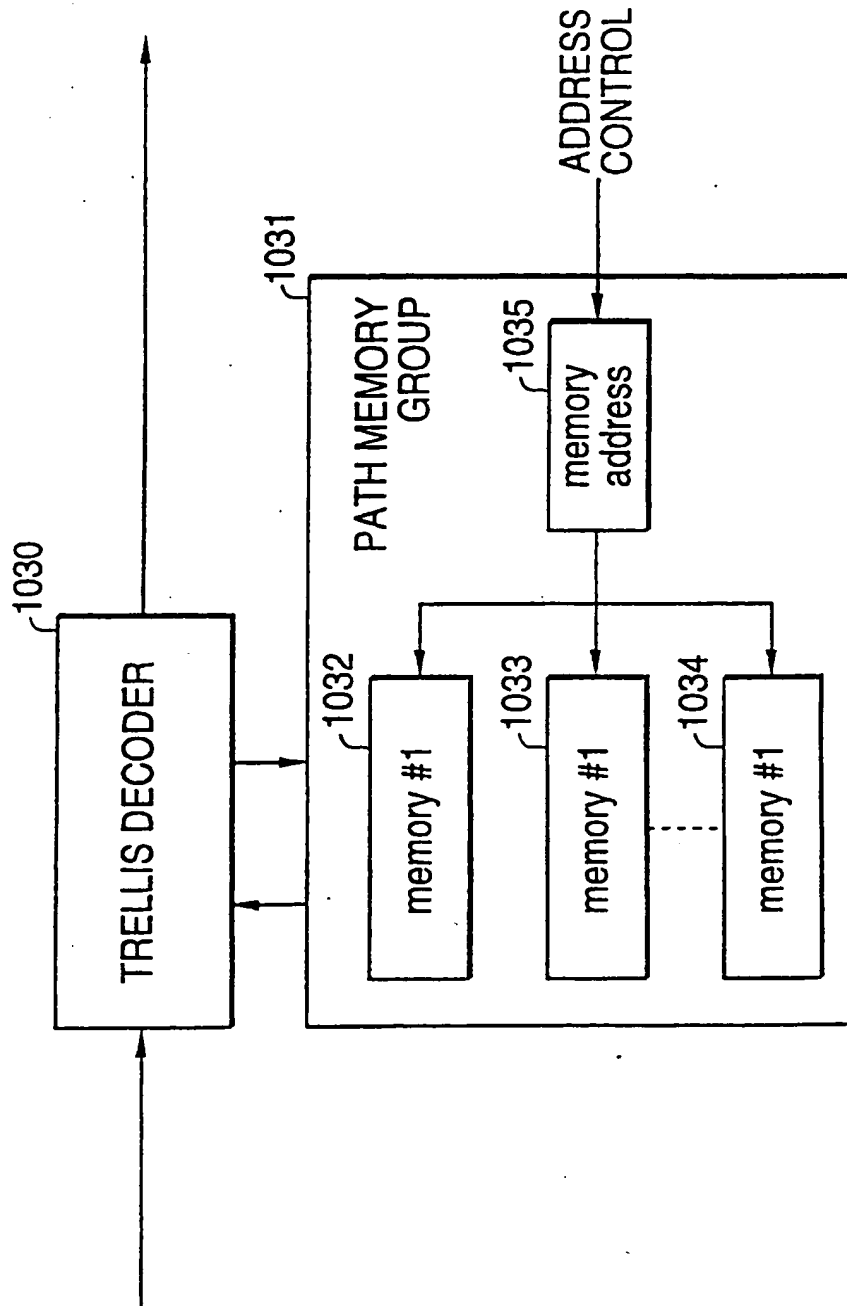


FIG. 178

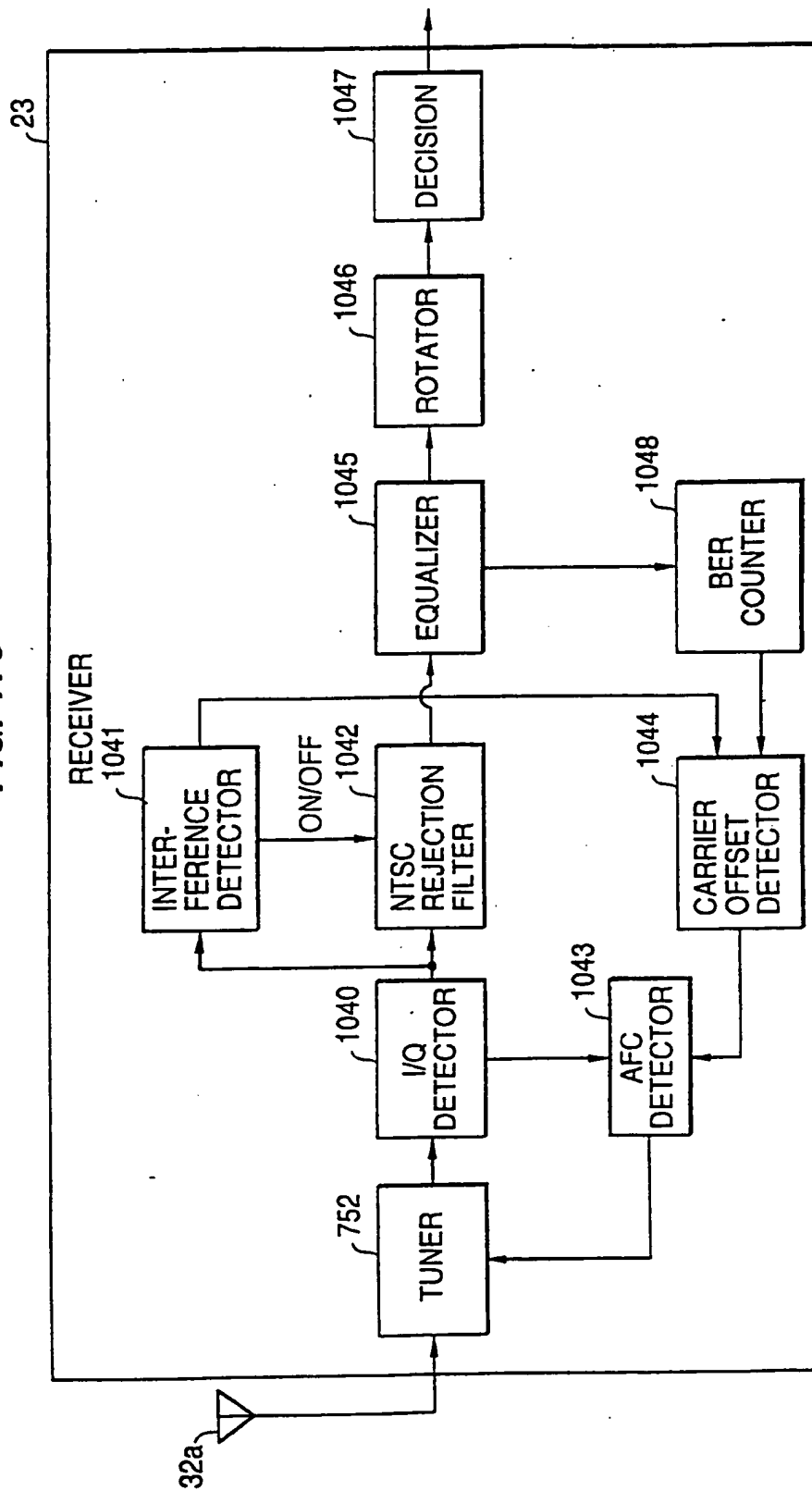


FIG. 179

